

Thorpe-2 TBT Logic Schematics

THP2 D-0
VER 0.01
Oct/26/2016

BASE LOGIC :
thp2_sitr_icfc_20161014

- | | | |
|------------------------------------|--------------------------------|-------------------------------------|
| 1.TITLE PAGE | 37.RJ45 CONNECTOR | 72.CHARGER SELECTOR |
| 2.EC HISTORY | 38.BLANK | 73.BLANK |
| 3.CPU(1/16) : DDI/EDP | 39.BLANK | 74.DC/DC VCC5M/VCC3M (TPS51285B-1) |
| 4.CPU(2/16) : DDR CHANNEL-A | 40.BLANK | 75.DC/DC IMVP8 CONTROLLER(NCP81218) |
| 5.CPU(3/16) : DDR CHANNEL-B | 41.BLANK | 76.DC/DC VCCCPUCORE(NCP81382) |
| 6.CPU(4/16) : MISC/JTAG | 42.BLANK | 77.DC/DC VCCGFXCORE_I(NCP81382) |
| 7.CPU(5/16) : LPC/SPI/SMBUS/C-LINK | 43.BLANK | 78.DC/DC VCCSA(NCP81380) |
| 8.CPU(6/16) : LPSS/ISH | 44.BLANK | 79.BLANK |
| 9.CPU(7/16) : AUDIO/SDXC | 45.BLANK | 80.DC/DC VCCCPUIO(NB682) |
| 10.CPU(8/16) : PCIE/USB/SATA | 46.PCIE M.2 (NGFF) CARD SLOT | 81.DC/DC VCC1R0_SUS(BD91364BMUU) |
| 11.CPU(9/16) : CSI-2/EMMC | 47.SD/AUDIO CONNECTOR I/F | 82.LOAD SW VCCST & VCCSTG |
| 12.CPU(10/16) : CLOCK SIGNALS | 48.BLANK | 83.DC/DC VCC1R2A(TPS51716RUKR) |
| 13.CPU(11/16) : SYSTEM PM | 49.BLANK | 84.BLANK |
| 14.CPU(12/16) : CPU POWER (1/2) | 50.AUDIO ALC3268 | 85.DC/DC VCC2R5A(TLV62080) |
| 15.CPU(13/16) : CPU POWER (2/2) | 51.AUDIO HP JACK DETECT | 86.DC/DC VCC1R8_SUS(BU90104GWZ) |
| 16.CPU(14/16) : PCH POWER | 52.AUDIO JACK SENSE | 87.DC/DC VCCPCHCORE(NB695) |
| 17.CPU(15/16) : GND | 53.BLANK | 88.BLANK |
| 18.CPU(16/16) : CFG/RESERVED | 54.AUDIO SPEAKER | 89.BLANK |
| 19.XDP CONNECTOR | 55.AUDIO BEEP | 90.BLANK |
| 20.RTC BATTERY | 56.BLANK | 91.BLANK |
| 21.SPI FLASH | 57.DOCKING CONNECTOR | 92.BLANK |
| 22.DDR4 BASE MEMORY CH-A (1/2) | 58.MEC1653(1/3) | 93.LOAD SW PCH SUS/TRACK POINT |
| 23.DDR4 BASE MEMORY CH-A (2/2) | 59.MEC1653(2/3) | 94.LOAD SW LAN |
| 24.DDR4 SO DIMM CHANNEL-B (1/2) | 60.MEC1653(3/3) | 95.BLANK |
| 25.DDR4 SO DIMM CHANNEL-B (2/2) | 61.KEYBOARD/TRACK POINT | 96.LOAD SW B |
| 26.LCD/USB/LID/MIC/CAMERA/PWR SW | 62.TOUCH PAD/FPR/SCR | 97.LOAD SW WWAN & WLAN |
| 27.BLANK | 63.FAN CONNECTOR | 98.BLANK |
| 28.BLANK | 64.APS G-SENSOR | 99.PTH FOR SCREW HOLES |
| 29.DDI DEMUX/HDMI LEVEL SHIFTER | 65.DISCRETE TPM 2.0 | 100. ALPINE RIDGE LP(1/2) |
| 30.HDMI CONNECTOR | 66.SMBUS SWITCH/LPC DEBUG PORT | 101. ALPINE RIDGE LP(2/2) |
| 31.M.2 SATA/PCIE SSD CARD SLOT | 67.THINK ENGINE-2(1/2) | 102. TBT PORT |
| 32.USB POWER/CONN | 68.THINK ENGINE-2(2/2) | 103. USB TYPE-C PROTOCTOR |
| 33.BLANK | 69.DC-IN | |
| 34.GBE JACKSONVILLE | 70.BATTERY INPUT | |
| 35.GBE LAN SWITCH | 71.BATTERY CHARGER(BQ25700) | |
| 36.GBE MAGNETICS | | |

EC HISTORY

CS15 THP2 D-0
(BASE LOGIC : thp2_sitr_lcfc_20161014)

VER.0.01 10/26/2016 APPLIED Power ECR10192016 / EC10242016

TABLE: Chip Capacitor Thermal Characteristics

		Code
-55 to 150degC -55 to 125degC	+/-30ppm/degC +/-30ppm/degC	NPO C0G
-55 to 125degC -55 to 105degC -55 to 85degC	+/-15% +/-22% +/-15%	X7R X6S X5R

TABLE: Chip Capacitor Tolerance

Tolerance	Code
+/-0.25pF +/-0.5pF	C D
+/-5% +/-10% +/-20% +80/-20%	J K M Z

TABLE: Chip Part Dimension

Size [mm]	mm Size Code	Inch Size Code
0.40 x 0.20 0.60 x 0.30 1.00 x 0.50 1.60 x 0.80 2.00 x 1.25 2.00 x 1.60 2.50 x 2.00 3.20 x 1.60 3.20 x 2.50 4.50 x 1.60 4.50 x 2.50 4.50 x 3.20 5.00 x 2.50 6.40 x 3.20	0402 0603 1005 1608 2125 2016 2520 3216 3225 4516 4525 4532 5025 6432	01005 0201 0402 0603 0805 0806 1008 1206 1210 1806 1810 1812 2010 2512

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LOGIC

	Pin	Interleave	Non-Interleave
Block 0	AL71	DDR0_DQ[0]	DDR0_DQ[0]
	AL68	DDR0_DQ[1]	DDR0_DQ[1]
	AN68	DDR0_DQ[2]	DDR0_DQ[2]
	AN69	DDR0_DQ[3]	DDR0_DQ[3]
	AL70	DDR0_DQ[4]	DDR0_DQ[4]
	AL69	DDR0_DQ[5]	DDR0_DQ[5]
	AN70	DDR0_DQ[6]	DDR0_DQ[6]
	AN71	DDR0_DQ[7]	DDR0_DQ[7]
	AR70	DDR0_DQ[8]	DDR0_DQ[8]
	AR68	DDR0_DQ[9]	DDR0_DQ[9]
	AU71	DDR0_DQ[10]	DDR0_DQ[10]
	AU68	DDR0_DQ[11]	DDR0_DQ[11]
	AR71	DDR0_DQ[12]	DDR0_DQ[12]
	AR69	DDR0_DQ[13]	DDR0_DQ[13]
AU70	DDR0_DQ[14]	DDR0_DQ[14]	
AU69	DDR0_DQ[15]	DDR0_DQ[15]	
Block 2	BB65	DDR0_DQ[16]	DDR0_DQ[32]
	AW65	DDR0_DQ[17]	DDR0_DQ[33]
	AW63	DDR0_DQ[18]	DDR0_DQ[34]
	AY63	DDR0_DQ[19]	DDR0_DQ[35]
	BA65	DDR0_DQ[20]	DDR0_DQ[36]
	AY65	DDR0_DQ[21]	DDR0_DQ[37]
	BA63	DDR0_DQ[22]	DDR0_DQ[38]
	BB63	DDR0_DQ[23]	DDR0_DQ[39]
	BA61	DDR0_DQ[24]	DDR0_DQ[40]
	AW61	DDR0_DQ[25]	DDR0_DQ[41]
	BB59	DDR0_DQ[26]	DDR0_DQ[42]
	AW59	DDR0_DQ[27]	DDR0_DQ[43]
	BB61	DDR0_DQ[28]	DDR0_DQ[44]
	AY61	DDR0_DQ[29]	DDR0_DQ[45]
BA59	DDR0_DQ[30]	DDR0_DQ[46]	
AY59	DDR0_DQ[31]	DDR0_DQ[47]	
Block 4	AY39	DDR0_DQ[32]	DDR1_DQ[0]
	AW39	DDR0_DQ[33]	DDR1_DQ[1]
	AY37	DDR0_DQ[34]	DDR1_DQ[2]
	AW37	DDR0_DQ[35]	DDR1_DQ[3]
	BB39	DDR0_DQ[36]	DDR1_DQ[4]
	BA39	DDR0_DQ[37]	DDR1_DQ[5]
	BA37	DDR0_DQ[38]	DDR1_DQ[6]
	BB37	DDR0_DQ[39]	DDR1_DQ[7]
	AY35	DDR0_DQ[40]	DDR1_DQ[8]
	AW35	DDR0_DQ[41]	DDR1_DQ[9]
	AY33	DDR0_DQ[42]	DDR1_DQ[10]
	AW33	DDR0_DQ[43]	DDR1_DQ[11]
	BB35	DDR0_DQ[44]	DDR1_DQ[12]
	BA35	DDR0_DQ[45]	DDR1_DQ[13]
BA33	DDR0_DQ[46]	DDR1_DQ[14]	
BB33	DDR0_DQ[47]	DDR1_DQ[15]	
Block 6	AY31	DDR0_DQ[48]	DDR1_DQ[32]
	AW31	DDR0_DQ[49]	DDR1_DQ[33]
	AY29	DDR0_DQ[50]	DDR1_DQ[34]
	AW29	DDR0_DQ[51]	DDR1_DQ[35]
	BB31	DDR0_DQ[52]	DDR1_DQ[36]
	BA31	DDR0_DQ[53]	DDR1_DQ[37]
	BA29	DDR0_DQ[54]	DDR1_DQ[38]
	BB29	DDR0_DQ[55]	DDR1_DQ[39]
	AY27	DDR0_DQ[56]	DDR1_DQ[40]
	AW27	DDR0_DQ[57]	DDR1_DQ[41]
	AY25	DDR0_DQ[58]	DDR1_DQ[42]
	BB27	DDR0_DQ[59]	DDR1_DQ[43]
	BA27	DDR0_DQ[60]	DDR1_DQ[44]
	BA25	DDR0_DQ[61]	DDR1_DQ[45]
BB25	DDR0_DQ[62]	DDR1_DQ[46]	
	DDR0_DQ[63]	DDR1_DQ[47]	



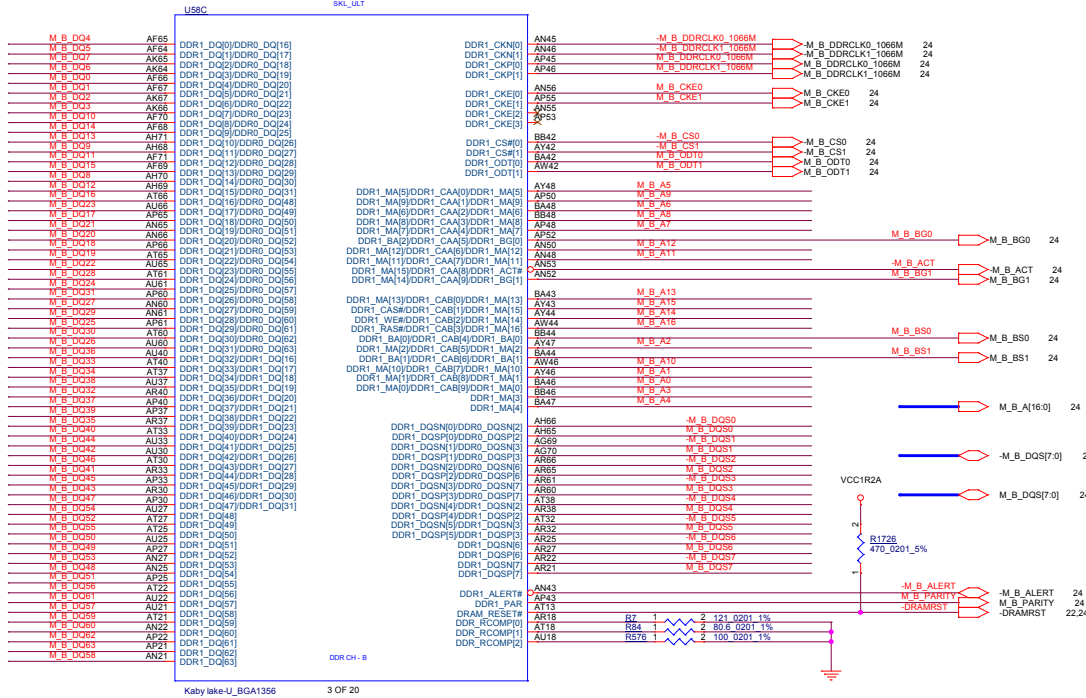
	Pin	Interleave	Non-Interleave
Block 0	AM70 AM69 AT69 AT70	DDR0_DQSN[0] DDR0_DQSP[0] DDR0_DQSN[1] DDR0_DQSP[1]	DDR0_DQSN[0] DDR0_DQSP[0] DDR0_DQSN[1] DDR0_DQSP[1]
Block 2	BA64 AY64 AY60 BA60	DDR0_DQSN[2] DDR0_DQSP[2] DDR0_DQSN[3] DDR0_DQSP[3]	DDR0_DQSN[4] DDR0_DQSP[4] DDR0_DQSN[5] DDR0_DQSP[5]
Block 4	BA38 AY38 AY34 BA34	DDR0_DQSN[4] DDR0_DQSP[4] DDR0_DQSN[5] DDR0_DQSP[5]	DDR1_DQSN[0] DDR1_DQSP[0] DDR1_DQSN[1] DDR1_DQSP[1]
Block 6	BA30 AY30 AY26 BA26	DDR0_DQSN[6] DDR0_DQSP[6] DDR0_DQSN[7] DDR0_DQSP[7]	DDR1_DQSN[4] DDR1_DQSP[4] DDR1_DQSN[5] DDR1_DQSP[5]



Pin	DDR3L	LPDDR3	DDR4
BA51	DDR0_MA[5]	DDR0_CAA[0]	DDR0_MA[5]
BB54	DDR0_MA[9]	DDR0_CAA[1]	DDR0_MA[9]
BA52	DDR0_MA[6]	DDR0_CAA[2]	DDR0_MA[6]
AY52	DDR0_MA[8]	DDR0_CAA[3]	DDR0_MA[8]
AW52	DDR0_MA[7]	DDR0_CAA[4]	DDR0_MA[7]
AY55	DDR0_BA[2]	DDR0_CAA[5]	DDR0_BG[0]
AW54	DDR0_MA[12]	DDR0_CAA[6]	DDR0_MA[12]
BA54	DDR0_MA[11]	DDR0_CAA[7]	DDR0_MA[11]
BA55	DDR0_MA[15]	DDR0_CAA[8]	DDR0_ACT#
AY54	DDR0_MA[14]	DDR0_CAA[9]	DDR0_BG[1]
AU46	DDR0_MA[13]	DDR0_CAB[0]	DDR0_MA[13]
AU48	DDR0_CAS#	DDR0_CAB[1]	DDR0_MA[15]
AT46	DDR0_WE#	DDR0_CAB[2]	DDR0_MA[14]
AU50	DDR0_RAS#	DDR0_CAB[3]	DDR0_MA[16]
AU52	DDR0_BA[0]	DDR0_CAB[4]	DDR0_BA[0]
AY51	DDR0_MA[2]	DDR0_CAB[5]	DDR0_MA[2]
AT48	DDR0_BA[1]	DDR0_CAB[6]	DDR0_BA[1]
AT50	DDR0_MA[10]	DDR0_CAB[7]	DDR0_MA[10]
BB50	DDR0_MA[1]	DDR0_CAB[8]	DDR0_MA[1]
AY50	DDR0_MA[0]	DDR0_CAB[9]	DDR0_MA[0]
BA50	DDR0_MA[3]	Not Used	DDR0_MA[3]
BB52	DDR0_MA[4]	Not Used	DDR0_MA[4]

	Pin	Interleave	Non-Interleave
Block 1	AF65	DDR1_DQ[0]	DDR0_DQ[16]
	AF64	DDR1_DQ[1]	DDR0_DQ[17]
	AK65	DDR1_DQ[2]	DDR0_DQ[18]
	AK64	DDR1_DQ[3]	DDR0_DQ[19]
	AF66	DDR1_DQ[4]	DDR0_DQ[20]
	AF67	DDR1_DQ[5]	DDR0_DQ[21]
	AK67	DDR1_DQ[6]	DDR0_DQ[22]
	AK66	DDR1_DQ[7]	DDR0_DQ[23]
	AF70	DDR1_DQ[8]	DDR0_DQ[24]
	AF68	DDR1_DQ[9]	DDR0_DQ[25]
	AH71	DDR1_DQ[10]	DDR0_DQ[26]
	AH68	DDR1_DQ[11]	DDR0_DQ[27]
	AF71	DDR1_DQ[12]	DDR0_DQ[28]
	AF69	DDR1_DQ[13]	DDR0_DQ[29]
	AH70	DDR1_DQ[14]	DDR0_DQ[30]
	AH69	DDR1_DQ[15]	DDR0_DQ[31]
Block 3	AT66	DDR1_DQ[16]	DDR0_DQ[48]
	AU66	DDR1_DQ[17]	DDR0_DQ[49]
	AP65	DDR1_DQ[18]	DDR0_DQ[50]
	AN65	DDR1_DQ[19]	DDR0_DQ[51]
	AN66	DDR1_DQ[20]	DDR0_DQ[52]
	AP66	DDR1_DQ[21]	DDR0_DQ[53]
	AT65	DDR1_DQ[22]	DDR0_DQ[54]
	AU65	DDR1_DQ[23]	DDR0_DQ[55]
	AT61	DDR1_DQ[24]	DDR0_DQ[56]
	AU61	DDR1_DQ[25]	DDR0_DQ[57]
	AP60	DDR1_DQ[26]	DDR0_DQ[58]
	AN60	DDR1_DQ[27]	DDR0_DQ[59]
	AN61	DDR1_DQ[28]	DDR0_DQ[60]
	AP61	DDR1_DQ[29]	DDR0_DQ[61]
	AT60	DDR1_DQ[30]	DDR0_DQ[62]
	AU60	DDR1_DQ[31]	DDR0_DQ[63]
Block 5	AU40	DDR1_DQ[32]	DDR1_DQ[16]
	AT40	DDR1_DQ[33]	DDR1_DQ[17]
	AT37	DDR1_DQ[34]	DDR1_DQ[18]
	AU37	DDR1_DQ[35]	DDR1_DQ[19]
	AP40	DDR1_DQ[36]	DDR1_DQ[20]
	AP37	DDR1_DQ[37]	DDR1_DQ[21]
	AR37	DDR1_DQ[38]	DDR1_DQ[22]
	AT33	DDR1_DQ[39]	DDR1_DQ[23]
	AU33	DDR1_DQ[40]	DDR1_DQ[24]
	AU30	DDR1_DQ[41]	DDR1_DQ[25]
	AT30	DDR1_DQ[42]	DDR1_DQ[26]
	AR33	DDR1_DQ[44]	DDR1_DQ[28]
	AP33	DDR1_DQ[45]	DDR1_DQ[29]
	AR30	DDR1_DQ[46]	DDR1_DQ[30]
	AP30	DDR1_DQ[47]	DDR1_DQ[31]
Block 7	AU27	DDR1_DQ[48]	DDR1_DQ[48]
	AT27	DDR1_DQ[49]	DDR1_DQ[49]
	AT25	DDR1_DQ[50]	DDR1_DQ[50]
	AU25	DDR1_DQ[51]	DDR1_DQ[51]
	AP27	DDR1_DQ[52]	DDR1_DQ[52]
	AN27	DDR1_DQ[53]	DDR1_DQ[53]
	AN25	DDR1_DQ[54]	DDR1_DQ[54]
	AP25	DDR1_DQ[55]	DDR1_DQ[55]
	AT22	DDR1_DQ[56]	DDR1_DQ[56]
	AU22	DDR1_DQ[57]	DDR1_DQ[57]
	AU21	DDR1_DQ[58]	DDR1_DQ[58]
	AT21	DDR1_DQ[59]	DDR1_DQ[59]
	AN22	DDR1_DQ[60]	DDR1_DQ[60]
	AP22	DDR1_DQ[61]	DDR1_DQ[61]
	AP21	DDR1_DQ[62]	DDR1_DQ[62]
	AN21	DDR1_DQ[63]	DDR1_DQ[63]

LOGIC



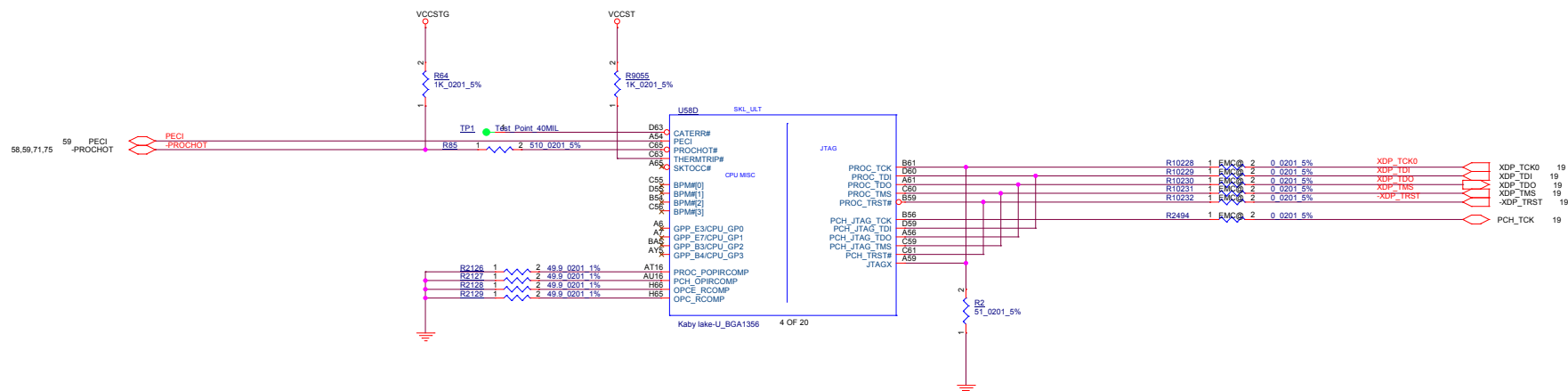
	Pin	Interleave	Non-Interleave
Block 1	AH66	DDR1_DQSN[0]	DDR0_DQSN[2]
	AG65	DDR1_DQSP[0]	DDR0_DQSP[2]
	AG69	DDR1_DQSN[1]	DDR0_DQSN[3]
	AG70	DDR1_DQSP[1]	DDR0_DQSP[3]
Block 3	AR66	DDR1_DQSN[2]	DDR0_DQSN[6]
	AR65	DDR1_DQSP[2]	DDR0_DQSP[6]
	AR64	DDR1_DQSN[3]	DDR0_DQSN[7]
	AR60	DDR1_DQSP[3]	DDR0_DQSP[7]
Block 5	AT38	DDR1_DQSN[4]	DDR1_DQSN[2]
	AR38	DDR1_DQSP[4]	DDR1_DQSP[2]
	AT32	DDR1_DQSN[5]	DDR1_DQSN[3]
	AR32	DDR1_DQSP[5]	DDR1_DQSP[3]
Block 7	AR25	DDR1_DQSN[6]	DDR1_DQSN[6]
	AR27	DDR1_DQSP[6]	DDR1_DQSP[6]
	AR22	DDR1_DQSN[7]	DDR1_DQSN[7]
	AR21	DDR1_DQSP[7]	DDR1_DQSP[7]

LOGIC

Pin	DDR3L	LPDDR3	DDR4
AY48	DDR1_MA[5]	DDR1_CAA[0]	DDR1_MA[5]
AP50	DDR1_MA[9]	DDR1_CAA[1]	DDR1_MA[9]
BA48	DDR1_MA[6]	DDR1_CAA[2]	DDR1_MA[6]
BB48	DDR1_MA[8]	DDR1_CAA[3]	DDR1_MA[8]
AP48	DDR1_MA[7]	DDR1_CAA[4]	DDR1_MA[7]
AP52	DDR1_BA[2]	DDR1_CAA[5]	DDR1_BG[0]
AN50	DDR1_MA[12]	DDR1_CAA[6]	DDR1_MA[12]
AN48	DDR1_MA[11]	DDR1_CAA[7]	DDR1_MA[11]
AN53	DDR1_MA[15]	DDR1_CAA[8]	DDR1_ACT#
AN52	DDR1_MA[14]	DDR1_CAA[9]	DDR1_BG[1]
BA43	DDR1_MA[13]	DDR1_CAB[0]	DDR1_MA[13]
AY43	DDR1_CAS#	DDR1_CAB[1]	DDR1_MA[15]
AY44	DDR1_WE#	DDR1_CAB[2]	DDR1_MA[14]
AW44	DDR1_RAS#	DDR1_CAB[3]	DDR1_MA[16]
BB44	DDR1_BA[0]	DDR1_CAB[4]	DDR1_BA[0]
AY47	DDR1_BA[2]	DDR1_CAB[5]	DDR1_BA[2]
BA44	DDR1_BA[1]	DDR1_CAB[6]	DDR1_BA[1]
AW46	DDR1_MA[10]	DDR1_CAB[7]	DDR1_MA[10]
AY46	DDR1_MA[1]	DDR1_CAB[8]	DDR1_MA[1]
BA46	DDR1_MA[0]	DDR1_CAB[9]	DDR1_MA[0]
BB46	DDR1_MA[3]	Not Used	DDR1_MA[3]
BA47	DDR1_MA[4]	Not Used	DDR1_MA[4]

LOGIC

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	CPU(3/6) : DDR CHANNEL-B	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.					
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SPI0_MOSI (Boot Halt)	
HIGH	Disabled (Default)
LOW	Enabled

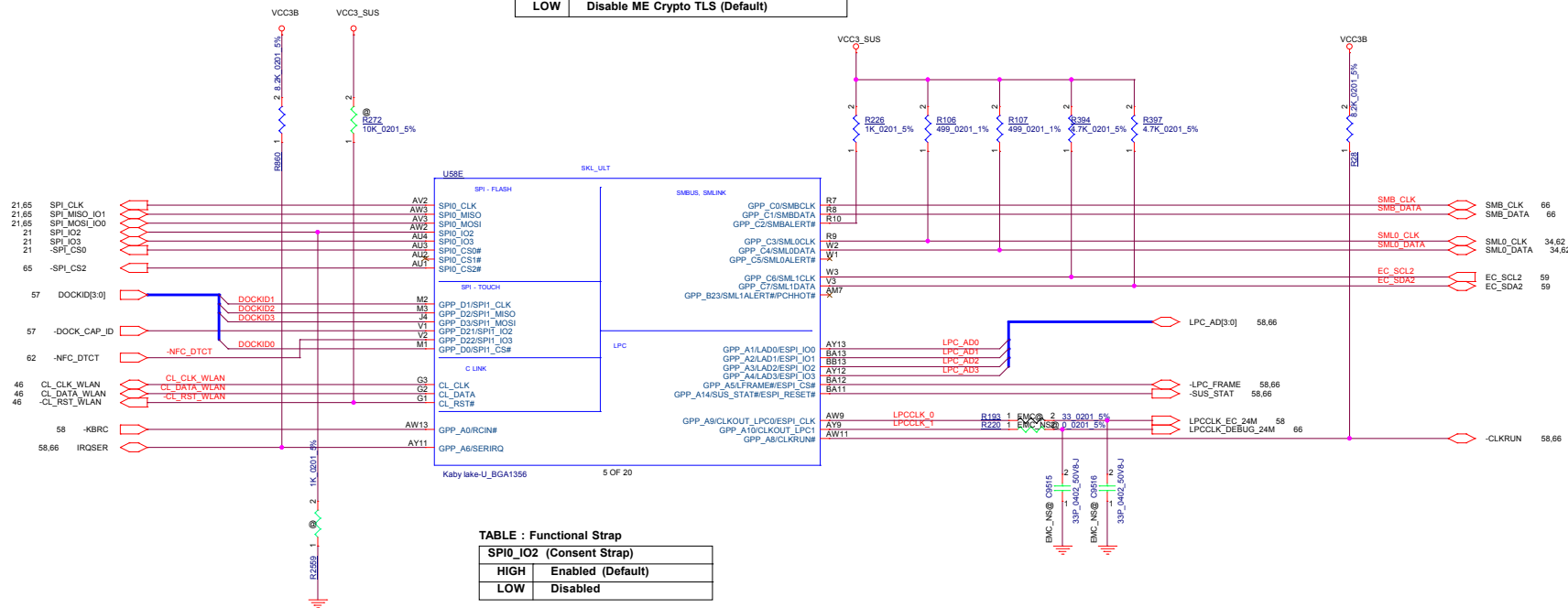
SPI0_MISO (JTAG ODT Disable)	
HIGH	Enabled (Default)
LOW	Disabled

GPP_C5/SML0ALERT # (LPC or eSPI)	
HIGH	eSPI is selected
LOW	LPC is selected (Default)

— LOGIC


GPP_C2/SMBALERT# (TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confidentiality
LOW	Disable ME Crypto TLS (Default)

LOGIC



SPI0_IO2 (Consent Strap)	
HIGH	Enabled (Default)
LOW	Disabled

SPI0_IO3 (A0 Personality Strap)	
HIGH	Disabled (Default)
LOW	Enabled

Security Classification	LC Future Center Secret Data			Title			
Issued Date	2012/07/01	Deciphered Date	2014/07/01	CU(5/16) : LPC/SP/SMBS/C-LINK			
<p>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF P&ID MANAGEMENT TO ANY OTHER DEPARTMENT OR AGENCY OF LC FUTURE CENTER WITHOUT THE WRITTEN CONSENT OF LC FUTURE CENTER. ANY INFORMATION CONTAINED HEREIN MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</p>					Size	Document Number	Rev
					Sheet	Thorse-2_UMA	0.01
					Date	Wednesday, October 24, 2012	1 of 103

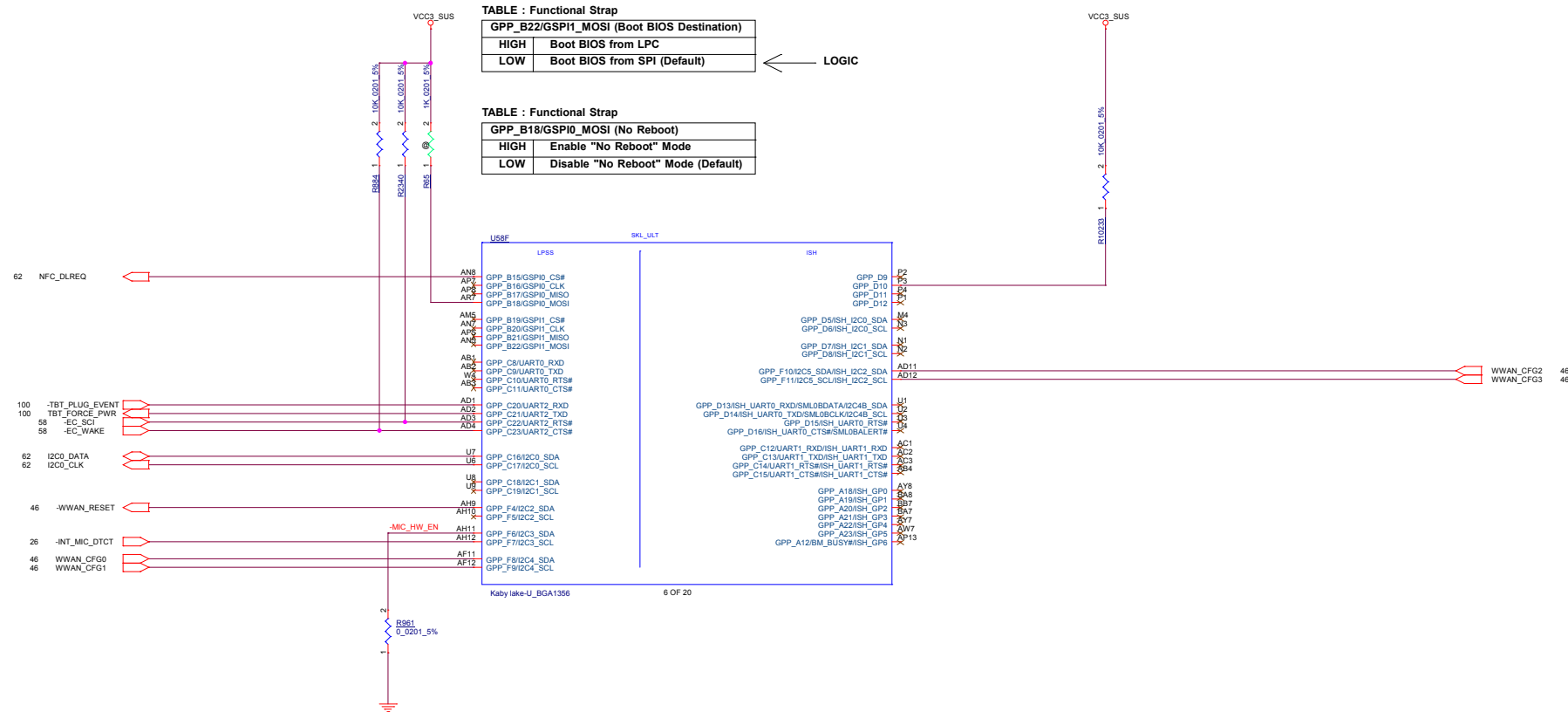


TABLE : Functional Strap

GPP_B22/GSPI1_MOSI (Boot BIOS Destination)	
HIGH	Boot BIOS from LPC
LOW	Boot BIOS from SPI (Default)

← LOGIC

TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)	
HIGH	Enable "No Reboot" Mode
LOW	Disable "No Reboot" Mode (Default)

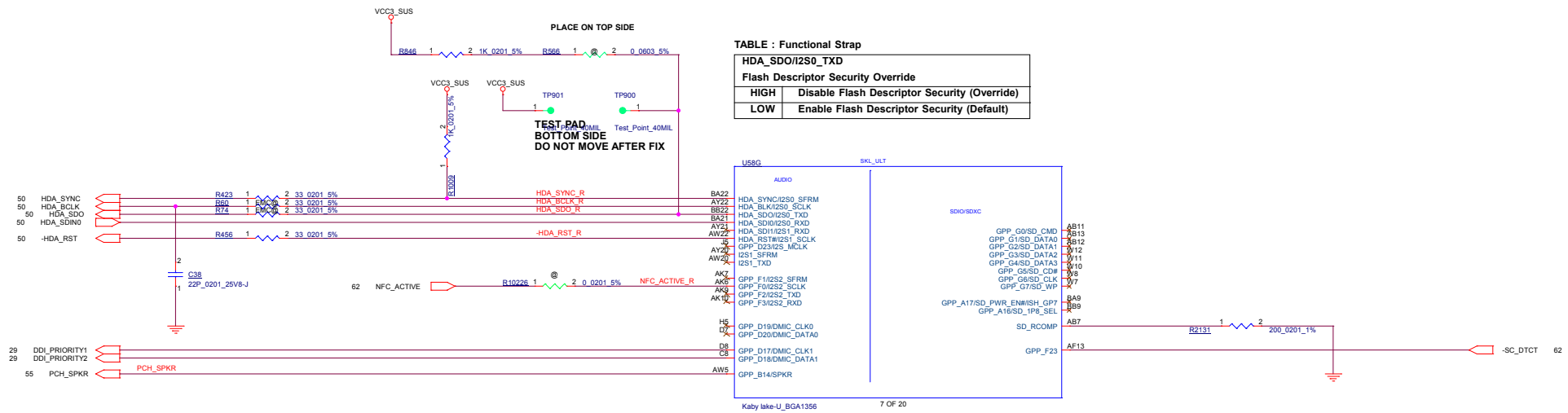


TABLE : Functional Strap

HDA_SDO/I2S0_TXD	
Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)

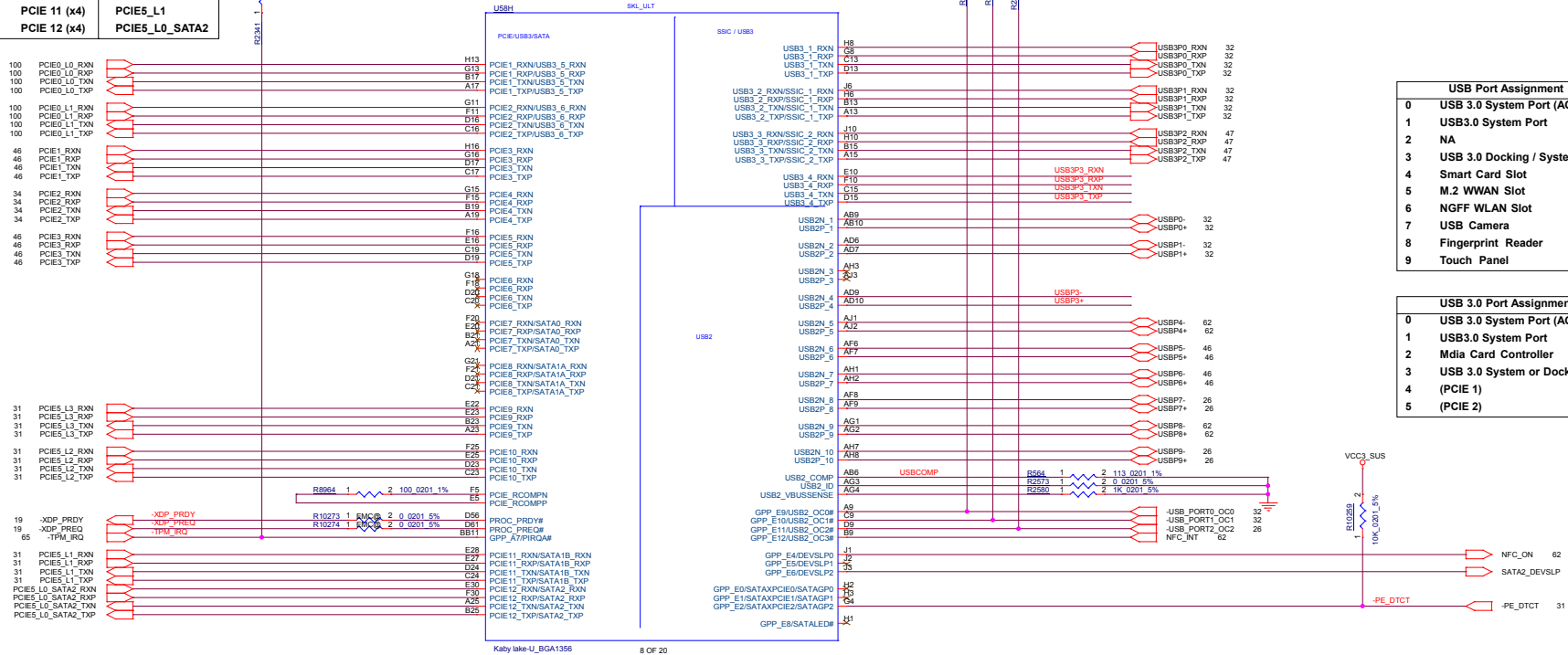
TABLE : Functional Strap

GPP_B14/SPKR (Top Swap Override)	
HIGH	Enable "Top Swap" Mode
LOW	Disable "Top Swap" Mode (Default)

Flexible I/O Configuration			
I/O	High Speed Signals	Configuration	Net Name
Port 1	USB3 1	USB3 1	USB3P0
Port 2	USB3 2/SSIC	USB3 2 (MCC)	USB3P1
Port 3	USB3 3	USB3 3	USB3P2
Port 4	USB3 4	USB3 4	USB3P3
Port 5	USB3 5/PCIE 1	PCIE 1 (x2)	PCIE0_L0
Port 6	USB3 6/PCIE 2	PCIE 2 (x2)	PCIE0_L1
Port 7	PCIE 3 (GbE)	PCIE 3	PCIE1
Port 8	PCIE 4 (GbE)	PCIE 4	PCIE2
Port 9	PCIE 5 (GbE)	PCIE 5	PCIE3
Port 10	PCIE 6	NA	X
Port 11	PCIE 7/SATA 0	NA	X
Port 12	PCIE 8/SATA 1A	NA	X
Port 13	PCIE 9 (GbE)	PCIE 9 (x4)	PCIE5_L3
Port 14	PCIE 10 (GbE)	PCIE 10 (x4)	PCIE5_L2
Port 15	PCIE 11/SATA 1B	PCIE 11 (x4)	PCIE5_L1
Port 16	PCIE 12/SATA 2	PCIE 12 (x4)	PCIE5_L0_SATA2

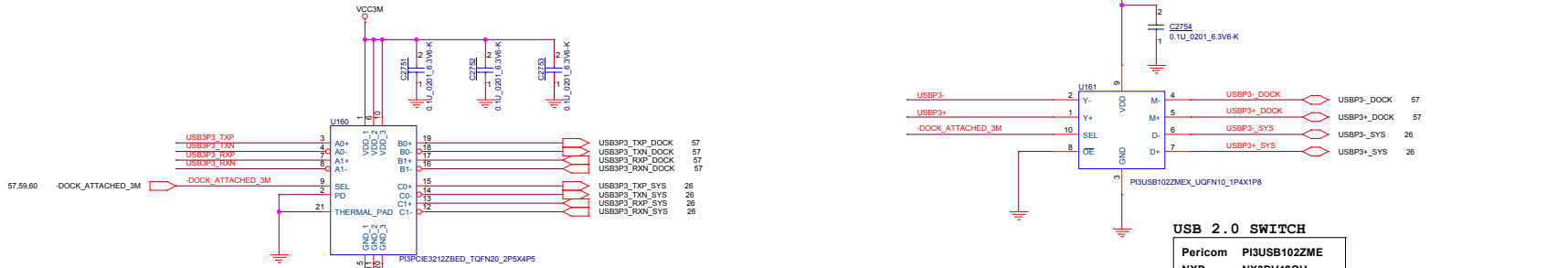
PCIe Port Assignment	
0 (x2)	Thunderbolt
1	M.2 WLAN Slot Port 0
2	GbE PHY
3	M.2 WLAN Slot Port 1
4 (x2)	NA
5 (x4)	PCIe SSD

SATA Port Assignment	
0 (PCIE 7)	
1A SATA SSD	
1B (PCIE 11)	
2 SATA SSD	



USB Port Assignment	
0	USB 3.0 System Port (AOU)
1	USB3.0 System Port
2	NA
3	USB 3.0 Docking / System Port (3rd Port)
4	Smart Card Slot
5	M.2 WWAN Slot
6	NGFF WLAN Slot
7	USB Camera
8	Fingerprint Reader
9	Touch Panel

USB 3.0 Port Assignment	
0	USB 3.0 System Port (AOU)
1	USB3.0 System Port
2	Media Card Controller
3	USB 3.0 System or DockingPort
4	(PCIE 1)
5	(PCIE 2)

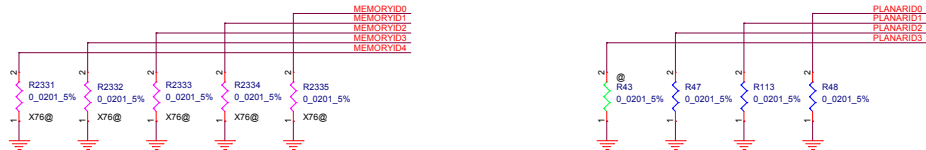


USB 3.0 MUX	
Pericom	P13PCIE3212ZBE
NXP	CBTL02043ABQ
NXP	CBTL02042ABQ

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Issued Date	2012/07/01	Deciphered Date	2014/07/01	CPU(8/16) : PCIE/USB/SATA	
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TABLE

MEMORYID[4..0]	U125, U126, U127, U128			
00000b	Micron	MT40A512M16HA-083E:A	8Gbit SDP	4GB (2133)
00001b	Micron	MT40A1G16HBA-083E:A	16Gbit DDP	8GB (2133)
00010b	Samsung	K4A8G165WB-BCPB	8Gbit SDP	4GB (2133)
00011b	SK Hynix	T.B.D.		
00100b	SK Hynix	T.B.D.		
01000b	Micron	MT40A512M16JY-083E:B	8Gbit SDP	4GB (2400)
01001b	Micron	MT40A1G16WBU-083E:B	16Gbit DDP	8GB (2400)
01010b	Samsung	K4A8G165WB-BCRC	8Gbit SDP	4GB (2400)
01011b	Samsung	K4AAG165WB-MCRC	16Gbit DDP	8GB (2400)
01100b	SK Hynix	H5AN8G6NAFR-UHC	8Gbit SDP	4GB (2400)
11111b	NO_ASM		No Soldered Memory	




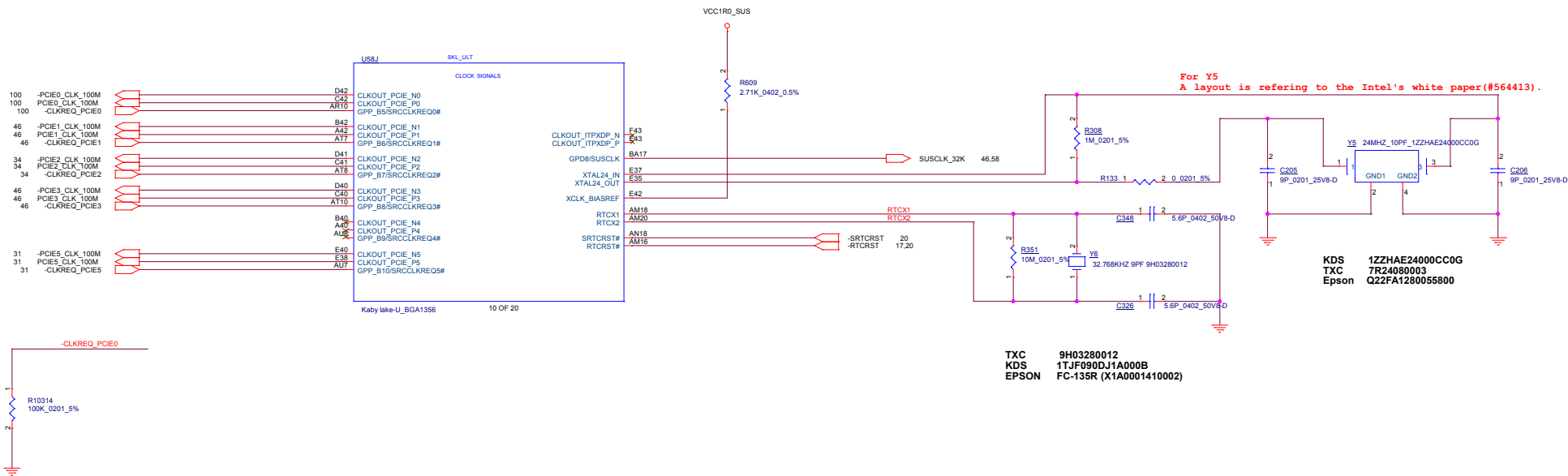
TABLE

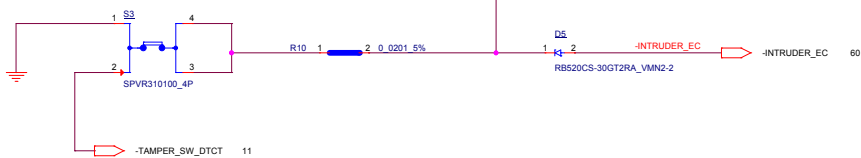
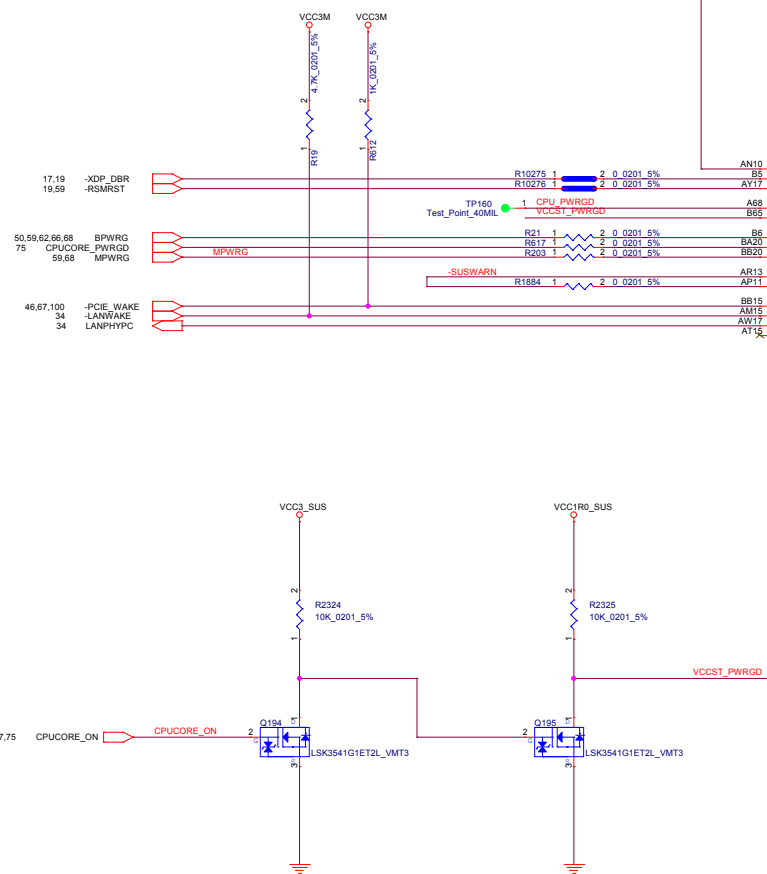
LEVEL	PLANAR ID			
	3	2	1	0
	R43	R47	R113	R48
1	NA	NA	NA	NA
0	ASM	ASM	ASM	ASM


TABLE

LEVEL	PLANARID[3..0]
PDV	0000B
SDV	0001B
FVT	0010B
ME SIT	0011B
SIT	0100B / 0101B
SIT-R	0110B / 0111B
SVT	1000B
SVT-R	
SOVP	

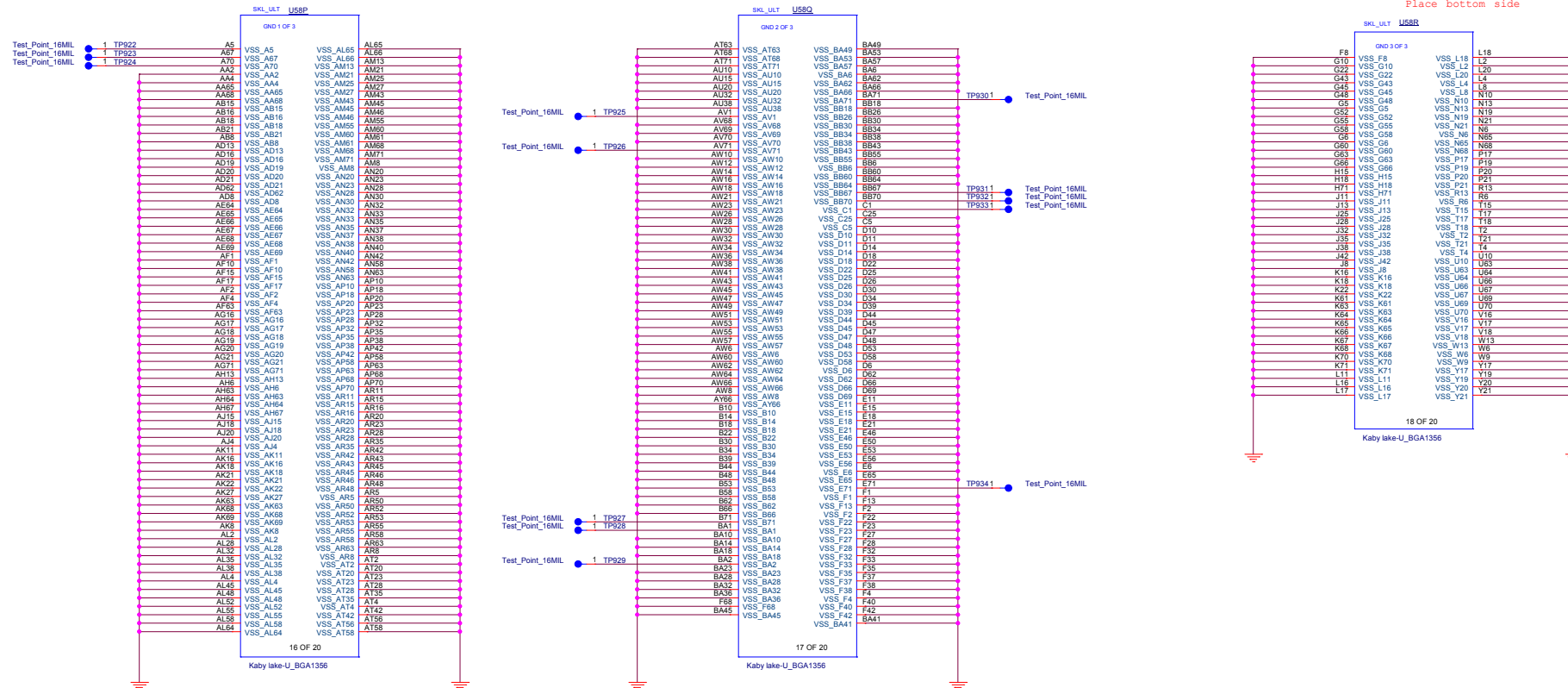
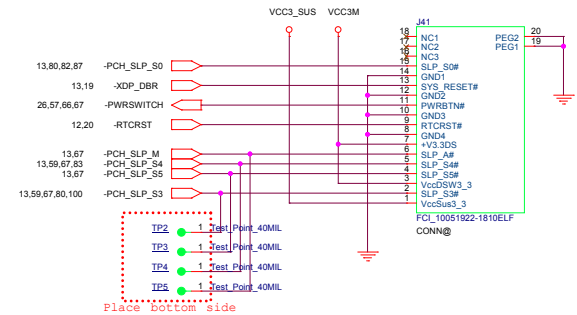
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Issued Date	2012/07/01	Deciphered Date	2014/07/01	CPU(9/16) : CSI-2/EMMC		
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									Date Wednesday, October 23, 2014 10:26 AM		Page 1 of 103			

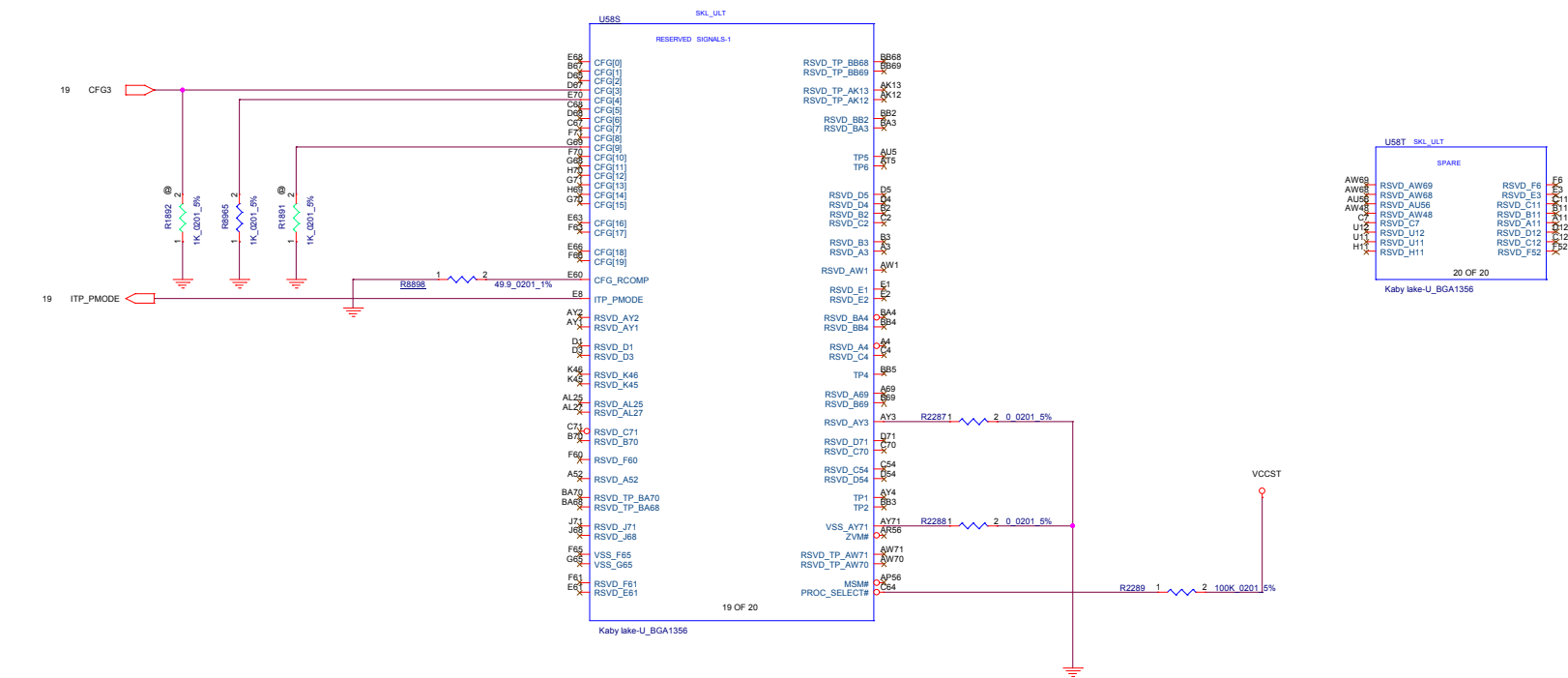
APS/PETS Interface

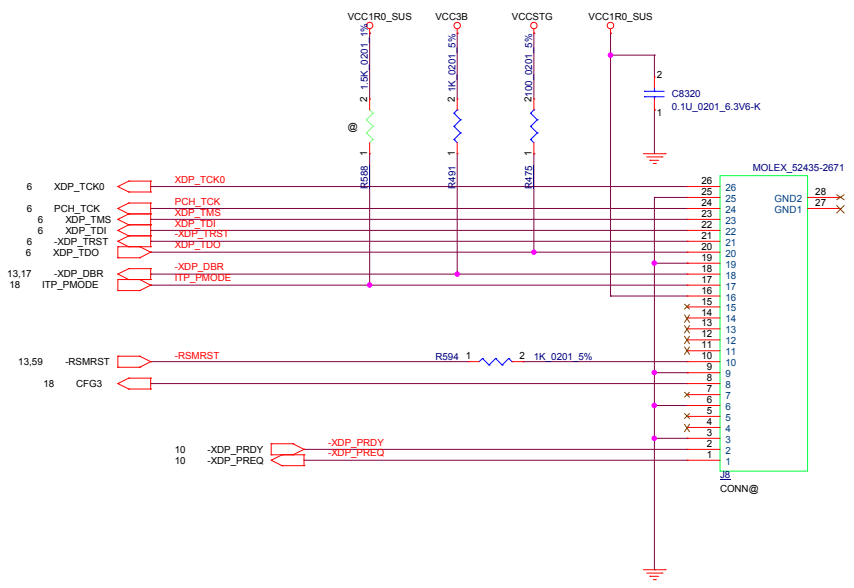


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TABLE

CFG0 : Stall Reset Sequence after PCU PLL Lock until de-asserted 1 : No Stall 0 : Stall
CFG3 : MSR Privacy Bit Feature 1 : MSR (C80h) bit[0] setting 0 : MSR (C80h) bit[0] overridden
CFG4 : eDP Enable 1 : Disabled 0 : Enabled
CFG9 : SVID Bus Communication 1 : Enabled 0 : Disabled

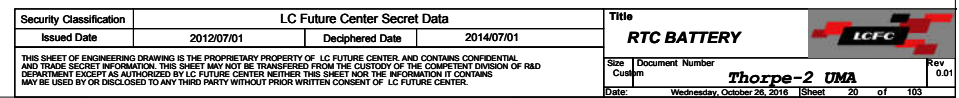


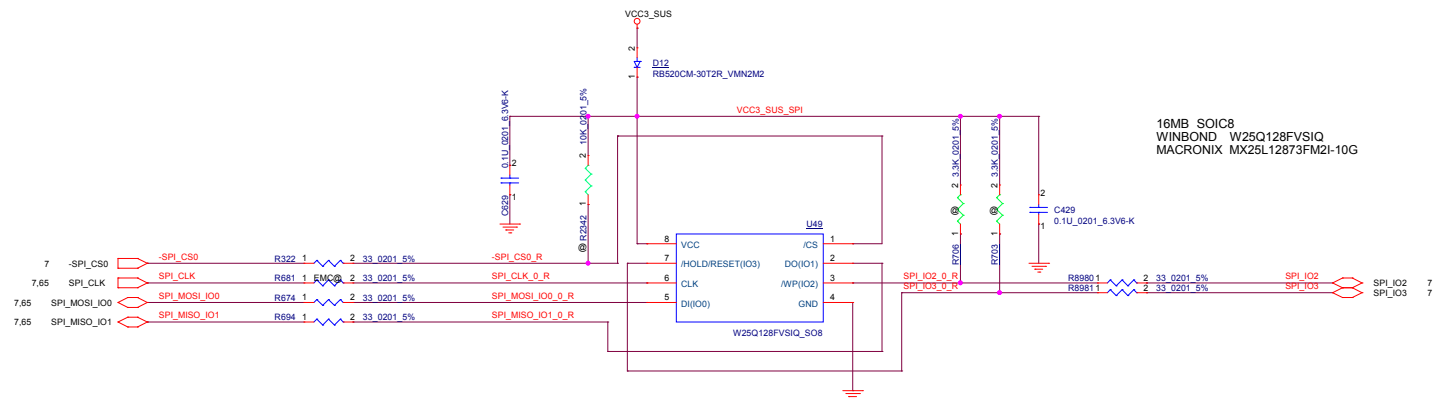


TABLE

Logic	Ref Des	Merged	DCI 2.0
Page 6	R2	ASM	ASM
Page 7	R2559	ASM	NO_ASM
Page 18	R1892	ASM	NO_ASM
Page 19	J8	ASM	NO_ASM
	C8320	ASM	NO_ASM
	R475	ASM	ASM
	R491	ASM	ASM
	R588	ASM	NO_ASM
	R594	ASM	NO_ASM
	R2494	ASM	NO_ASM

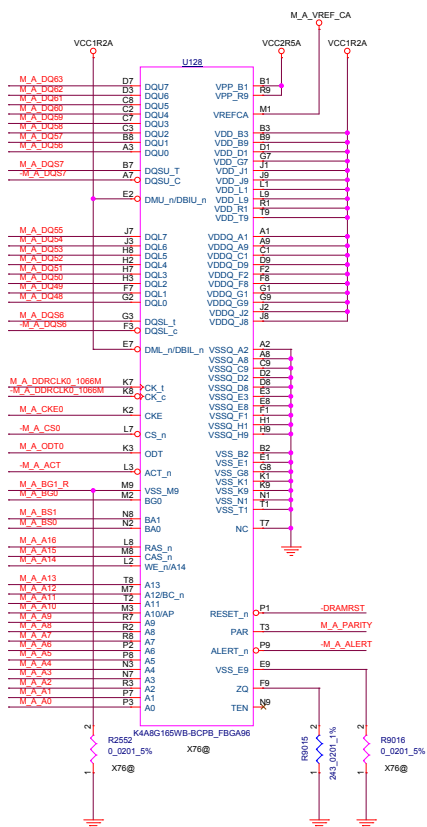
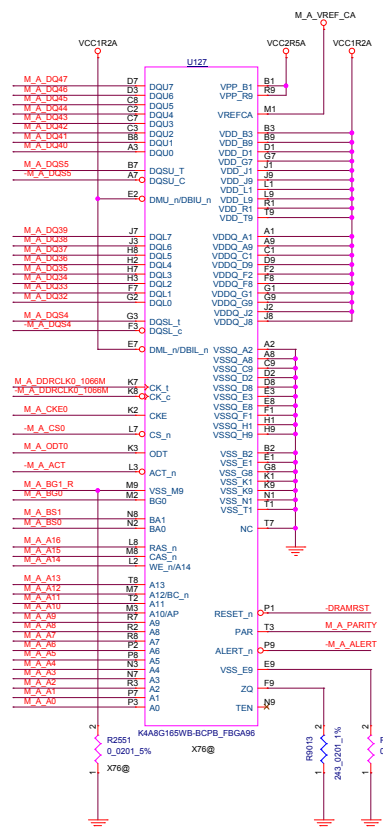
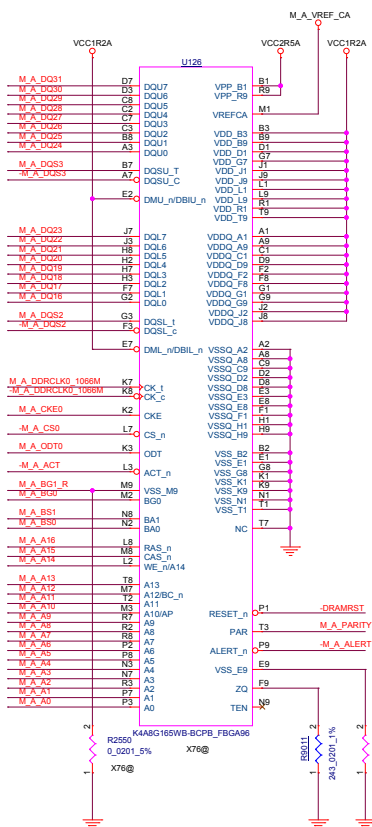
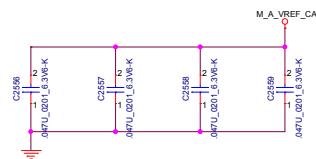
↑
LOGIC



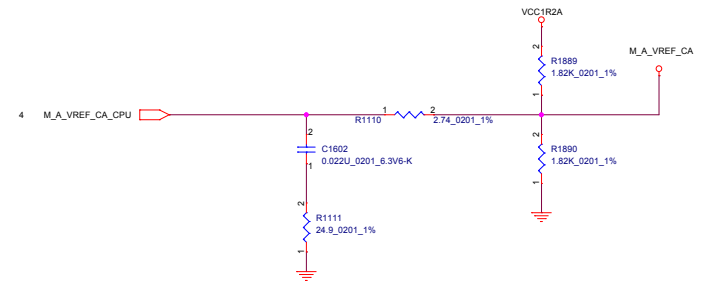
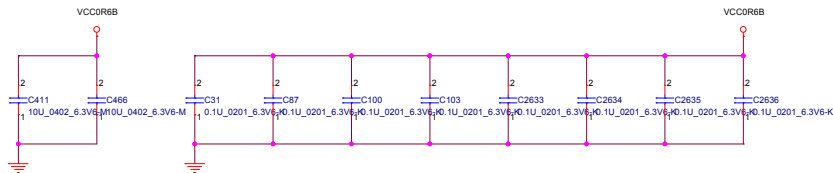
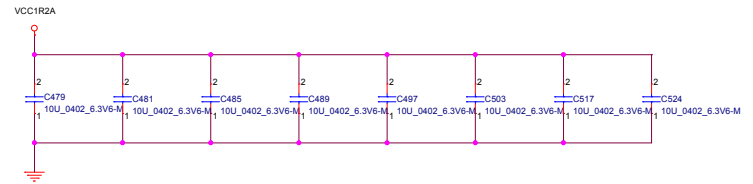
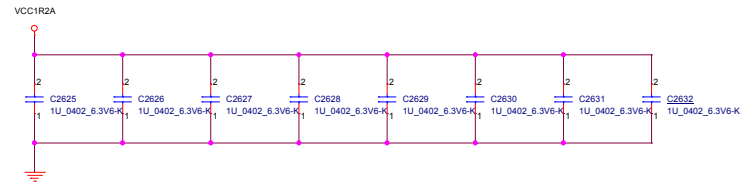
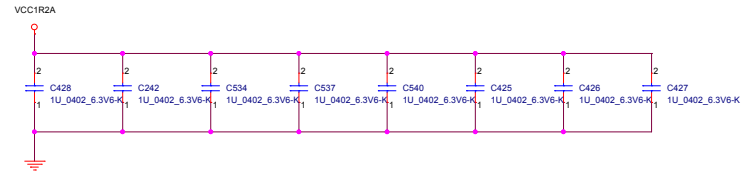
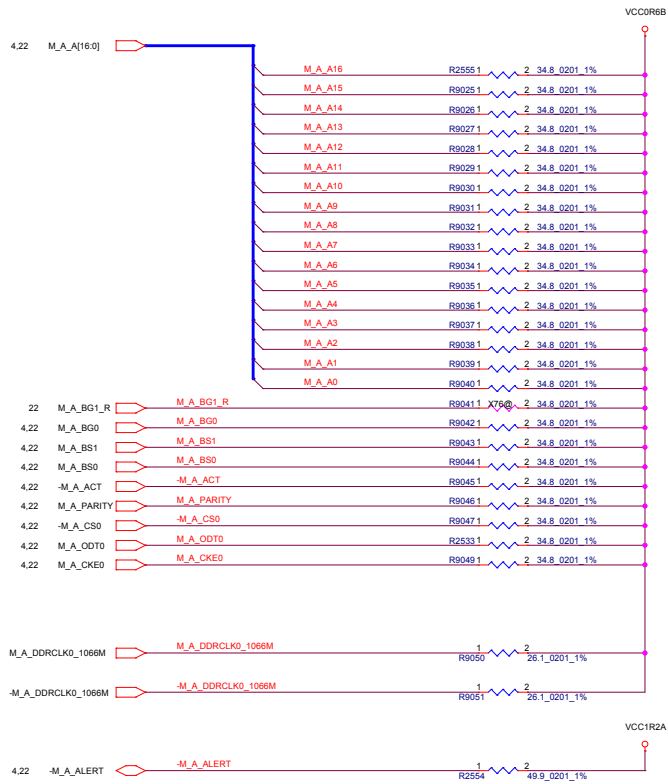


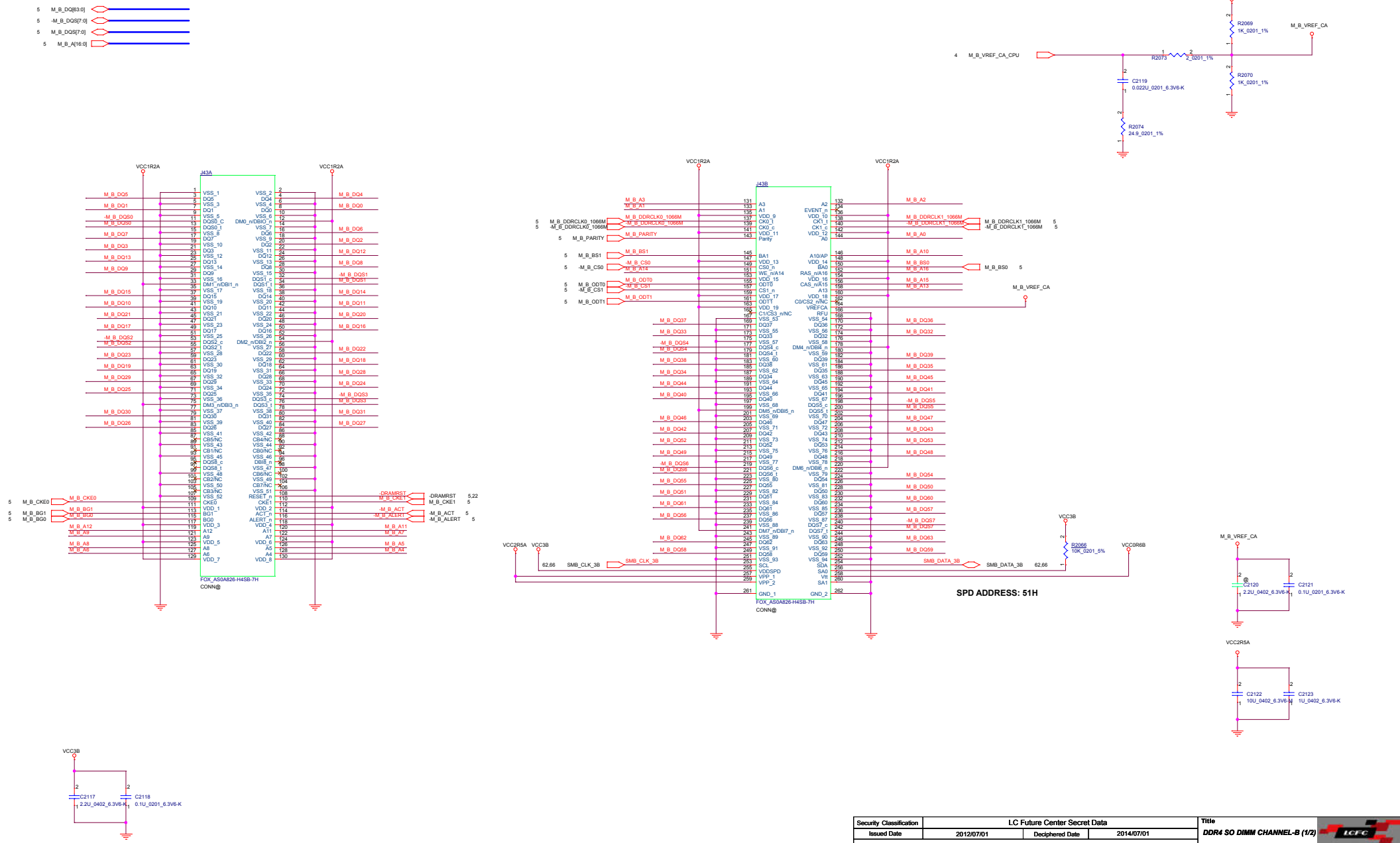
TABLE

SF100 PIN HEADER INTERFACE (TOP VIEW)							
1	VCC	D12.1	GND	GND	2		
3	CS#	R322.2	GND	R681.2	CLK	4	
5	MISO	R694.2	N/A	R674.2	MOSI	6	
7	(KEY)	N/A	N/A		(RESET)	8	

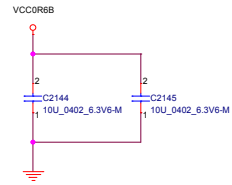
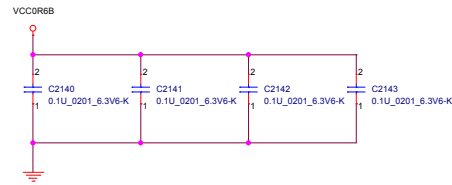
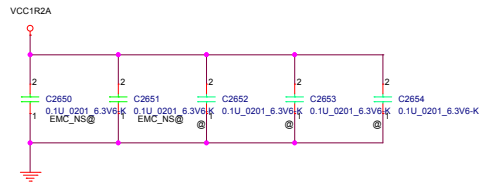
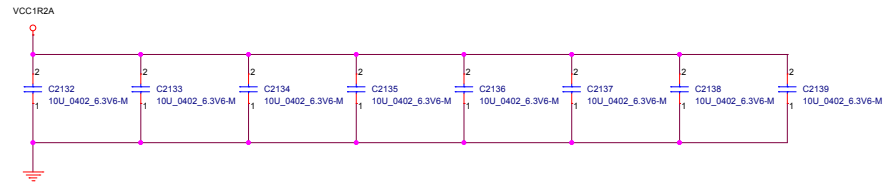
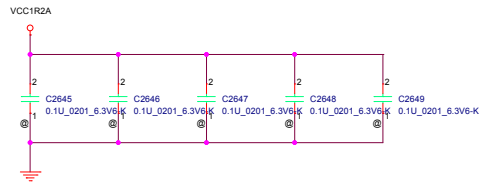
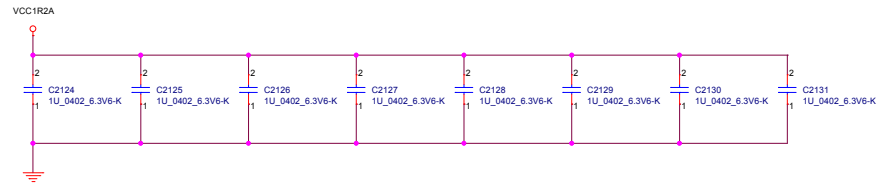
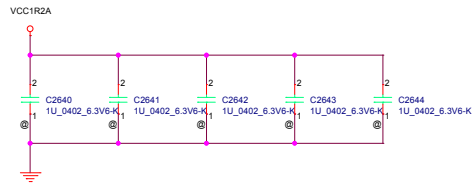


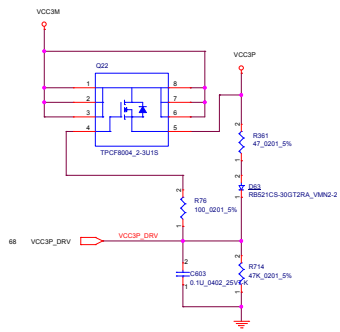
The schematic diagram illustrates the M_A_DORCLK0_1066M circuit. It features a 0.020 1% resistor (R2553) and a 0.1u 0201_6.3V6-K capacitor (C1063). The circuit is connected to several signals: M_A_DORCLK0_1066M, M_A_BG1, M_A_BG1_R, M_A_ALERT, M_A_PARITY, and DRAMRST. The circuit is powered by a 3V6-K supply.



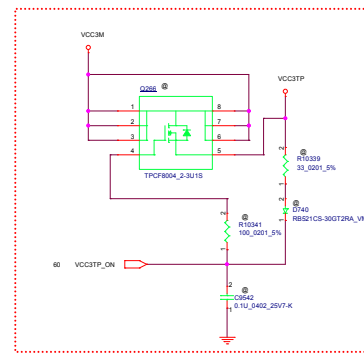


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		Sheet		24 of 103	

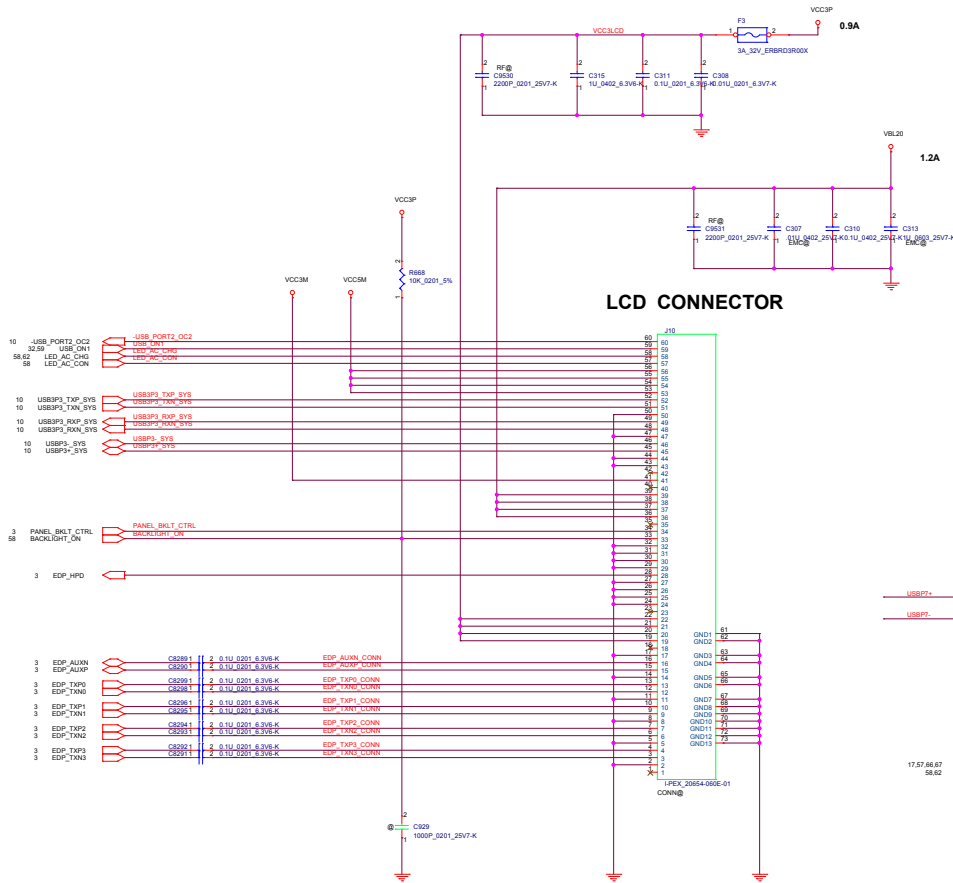
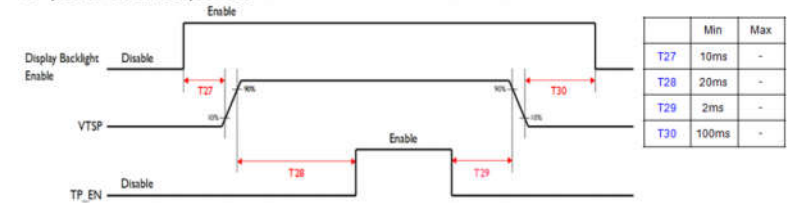




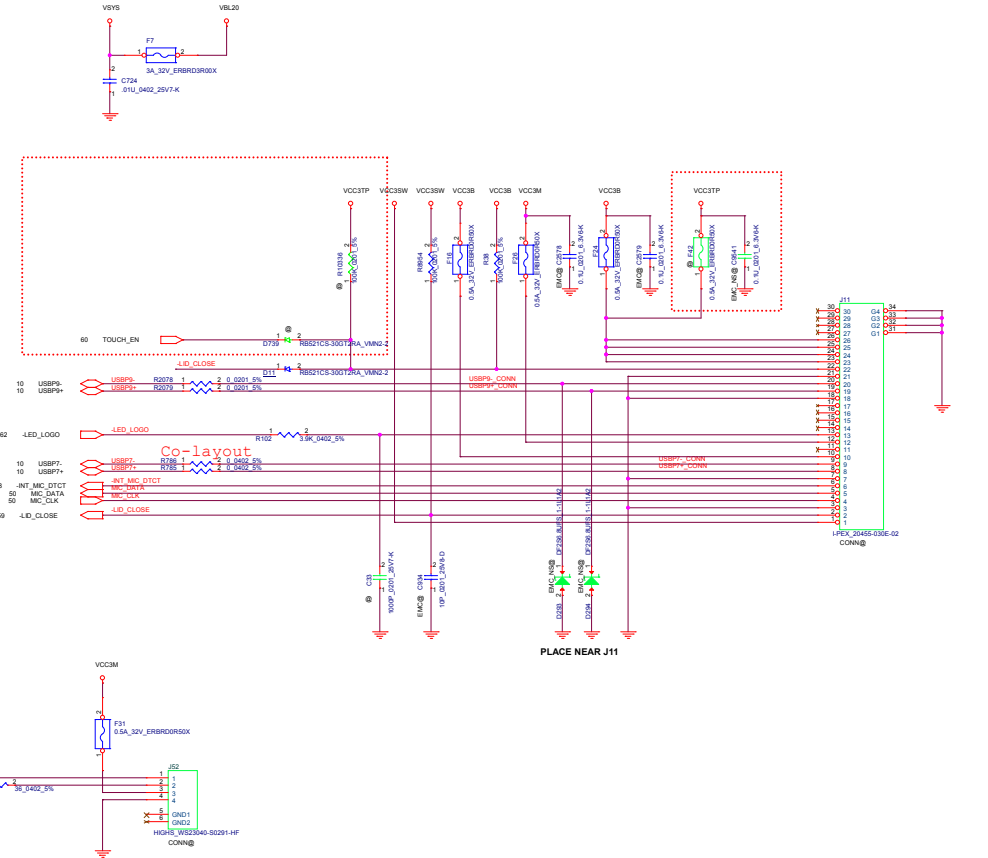
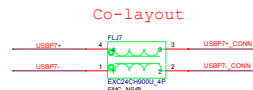
	Touch Panel		Sequence
	Support	Non-Support	
X10380	ASX	No ASX	
F42	ASX	No ASX	
D739	ASX	No ASX	
C0641	ASX	No ASX	
Q266	ASX	No ASX	
X10941	ASX	No ASX	
C0642	ASX	No ASX	
X10950	ASX	No ASX	
D740	ASX	No ASX	
X10957	ASX	No ASX	
X10958	ASX	No ASX	
X28	No ASX	ASX	
F54	No ASX	ASX	
X10959	No ASX	ASX	
X2412	No ASX	ASX	



TP power on/off Sequence:




LCD CONNECTOR



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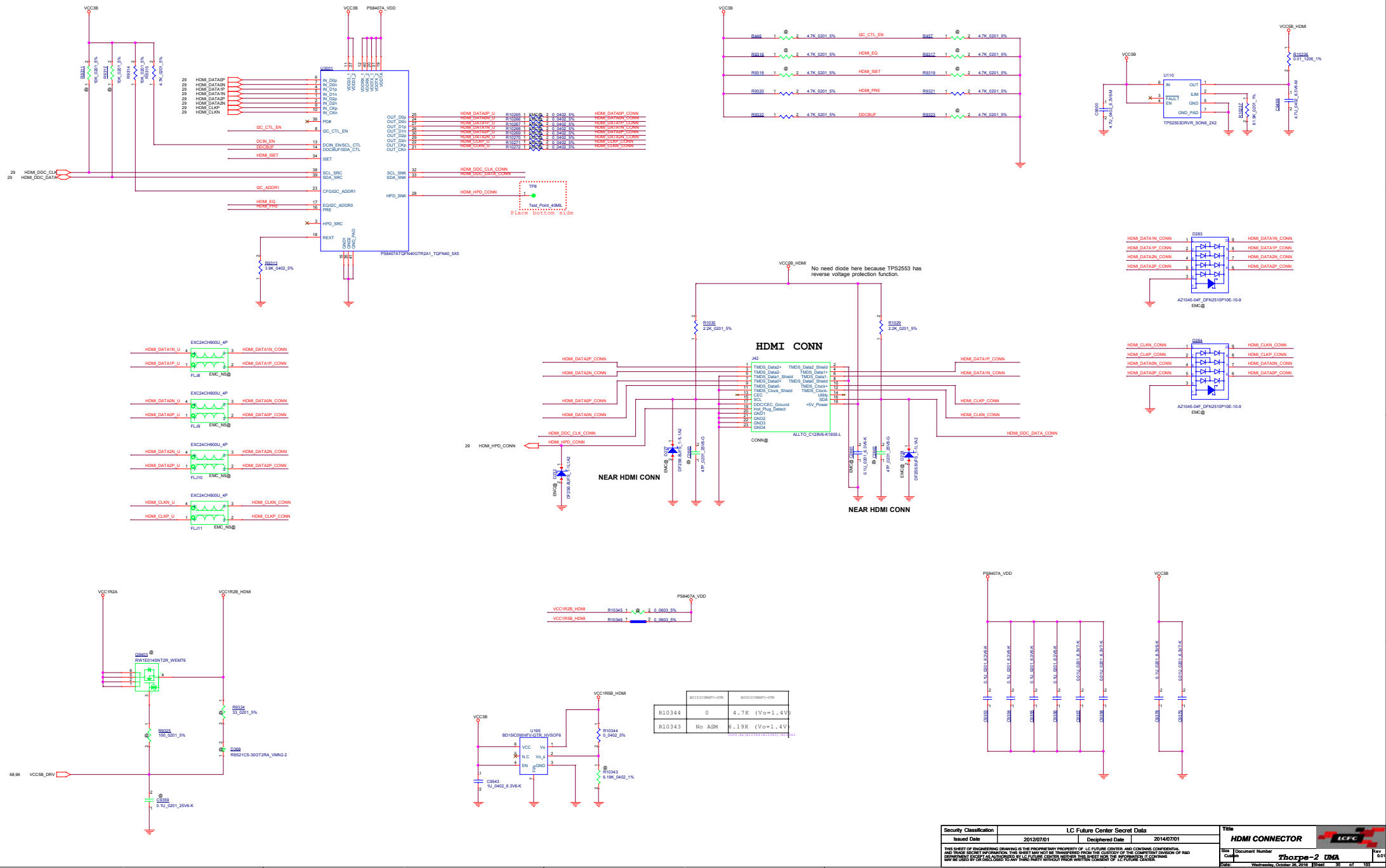
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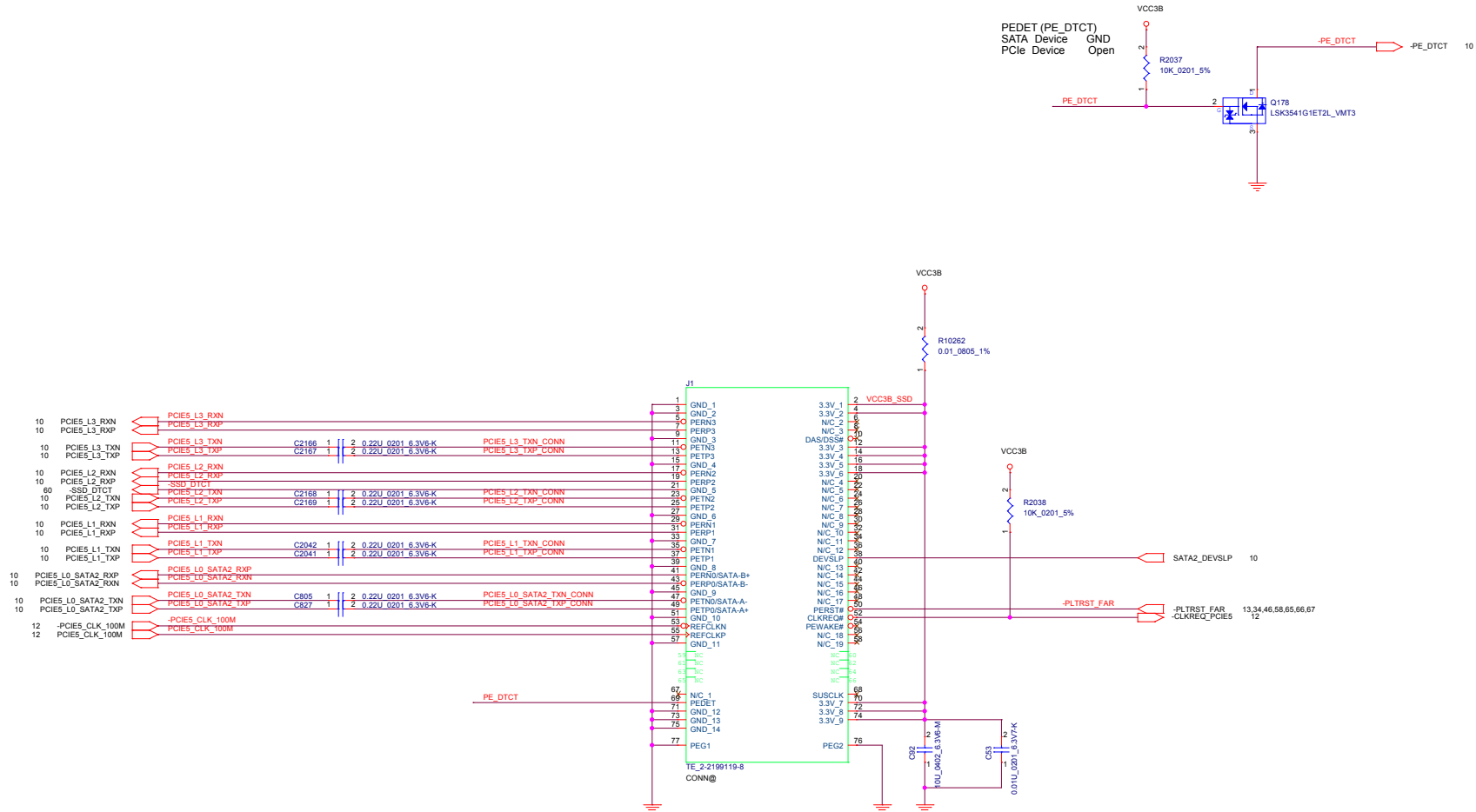


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				Document Number Rev 0.01	
				Date: Wednesday, October 26, 2016 Sheet 28 of 103	




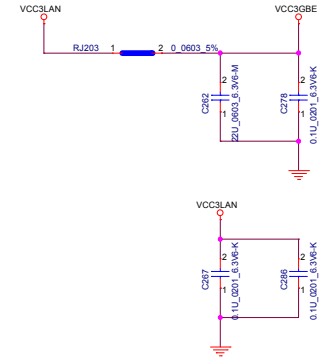
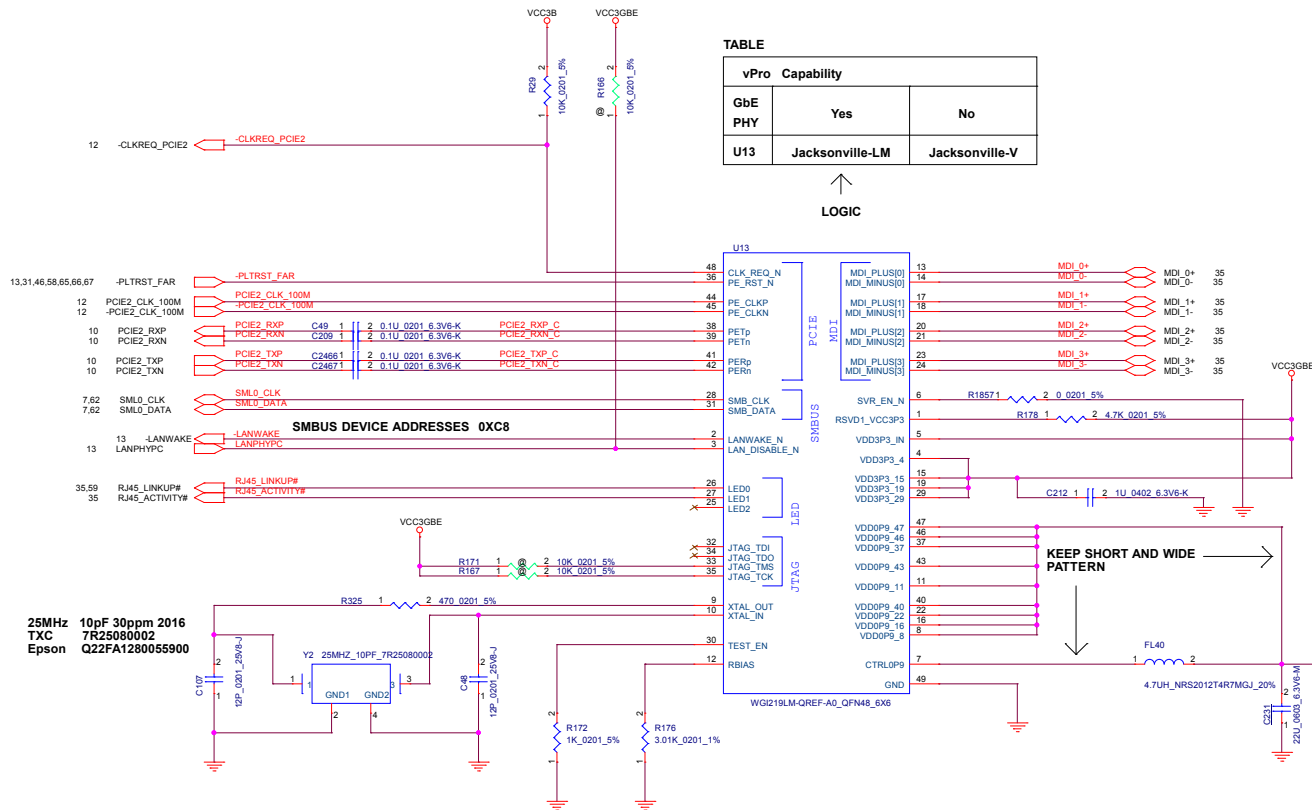




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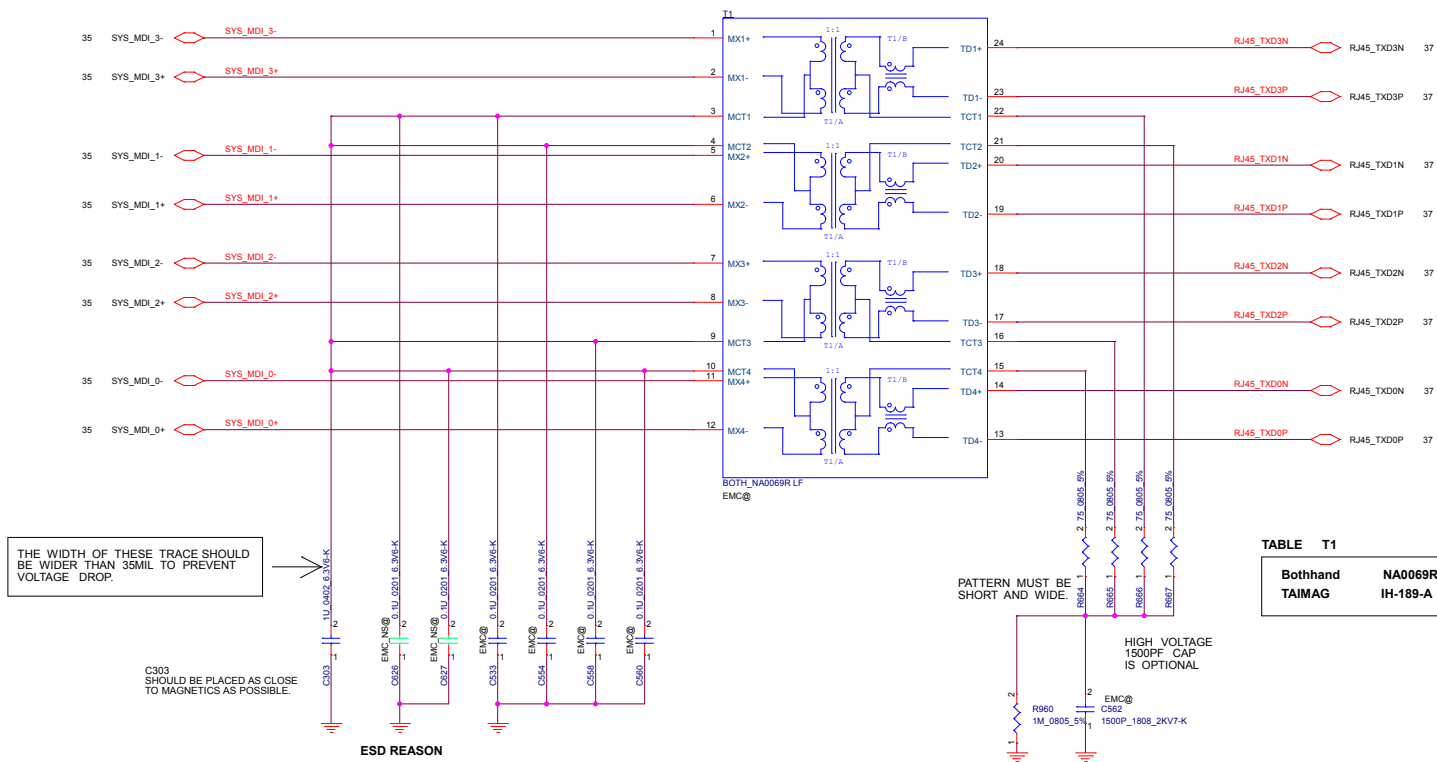
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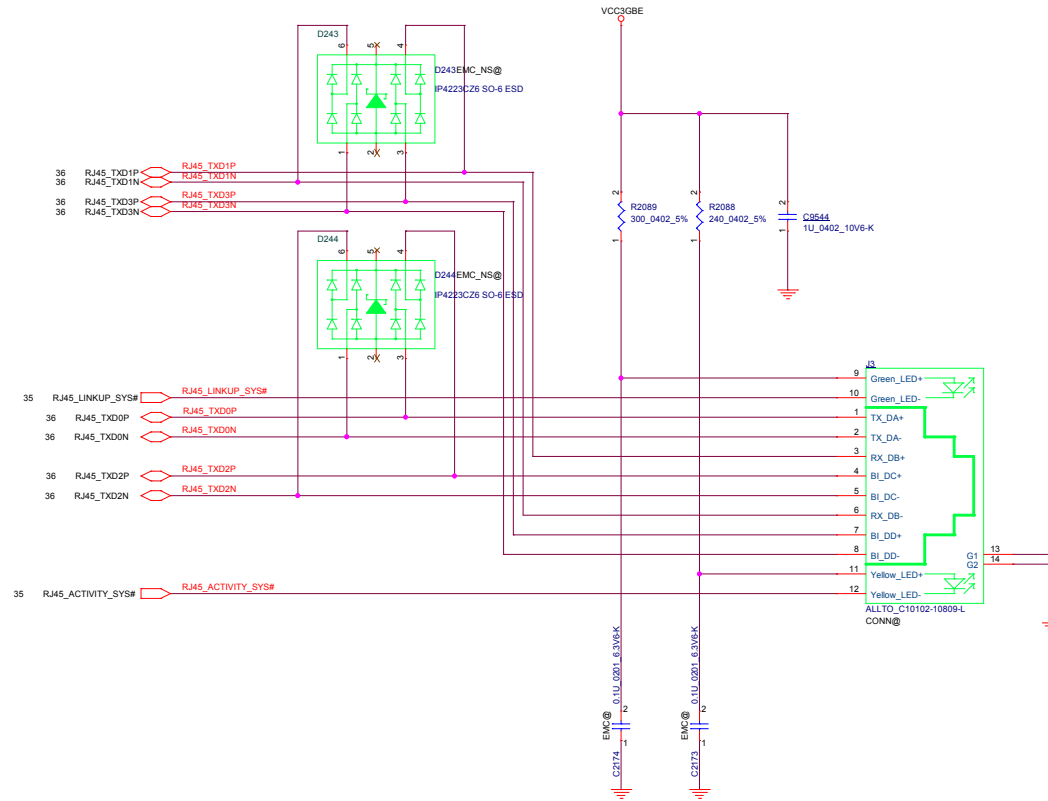




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								Date		Wednesday, October 26, 2016		Sheet 34 of 103	

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Size Custom					Thorpe-2 UMA
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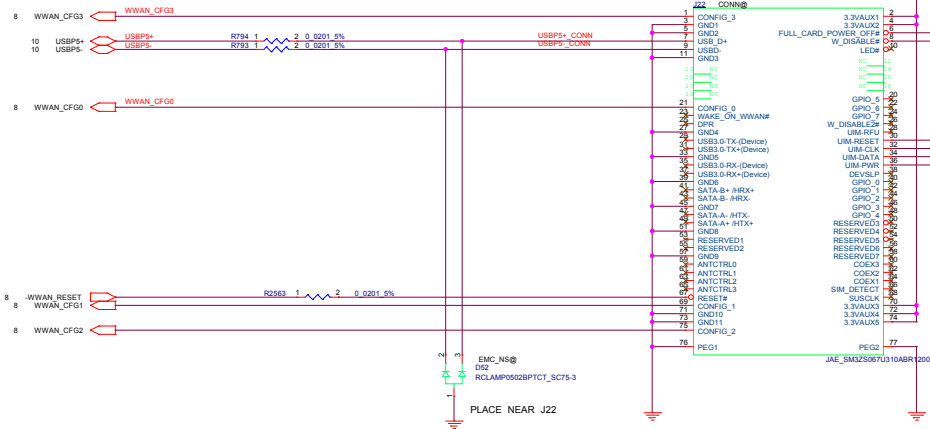
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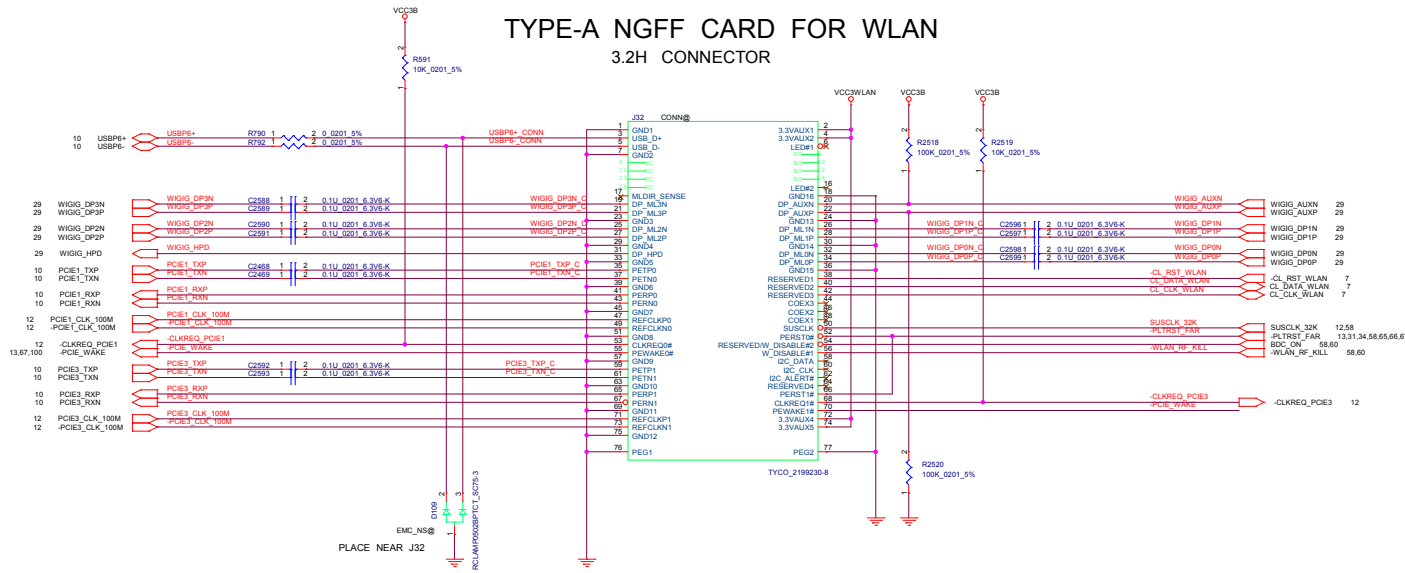
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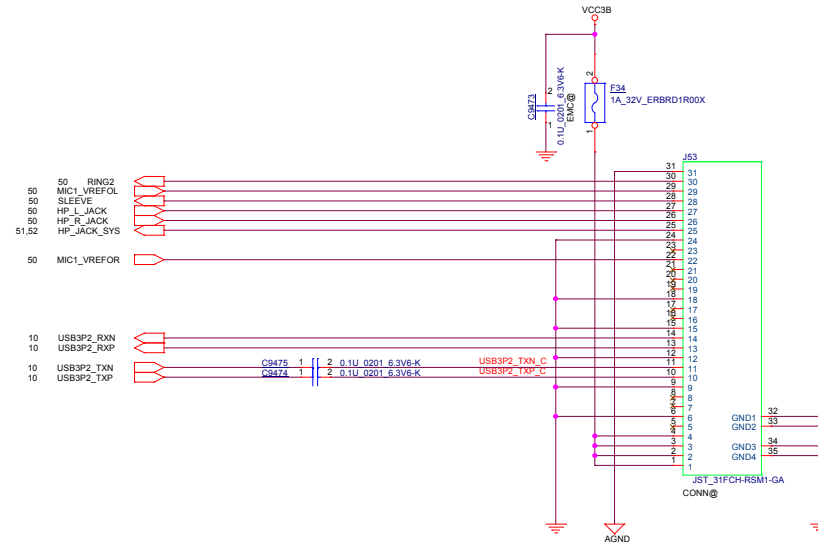
[illegible]

The figure displays three circuit diagrams, each representing a different parasitic capacitance value in the implementation of a 100pF capacitor using a 100nF capacitor and a 100k resistor in parallel.

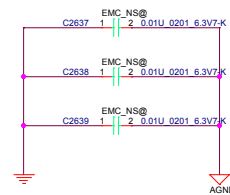
- Top Diagram (0.1pF parasitic):** Shows a 100nF capacitor (C103) in parallel with a 100k resistor (R100). The parasitic capacitance is 0.1pF. The total capacitance is 100.001pF. The component values are: C103 = 100nF, R100 = 100k, C118 = 0.1pF, C119 = 10.0002pF, C1156 = 100.001pF.
- Middle Diagram (0.2pF parasitic):** Shows a 100nF capacitor (C103) in parallel with a 100k resistor (R100). The parasitic capacitance is 0.2pF. The total capacitance is 100.002pF. The component values are: C103 = 100nF, R100 = 100k, C116 = 0.2pF, C117 = 10.0002pF, C1155 = 100.002pF.
- Bottom Diagram (0.5pF parasitic):** Shows a 100nF capacitor (C103) in parallel with a 100k resistor (R100). The parasitic capacitance is 0.5pF. The total capacitance is 100.005pF. The component values are: C103 = 100nF, R100 = 100k, C2005 = 0.5pF, C2007 = 10.0002pF, C2008 = 100.005pF.



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Reserved for EMC/RF solution



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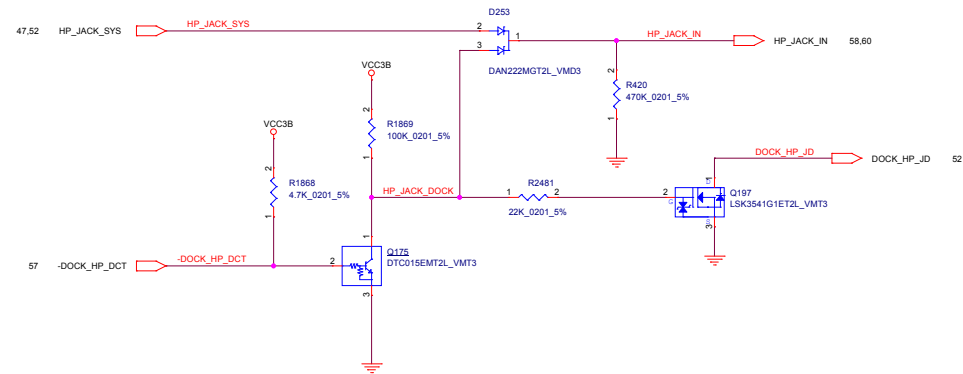
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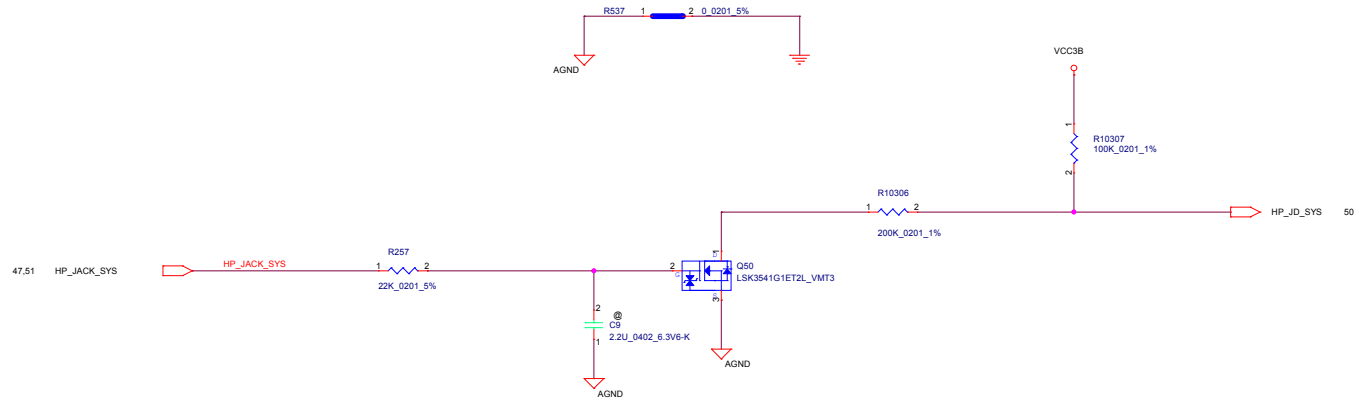


TABLE

DOCKING	SUPPORT	NON-SUPPORT
R1869	ASM	NO_ASM
Q175	ASM	NO_ASM
R2481	ASM	NO_ASM
Q197	ASM	NO_ASM

↑
LOGIC

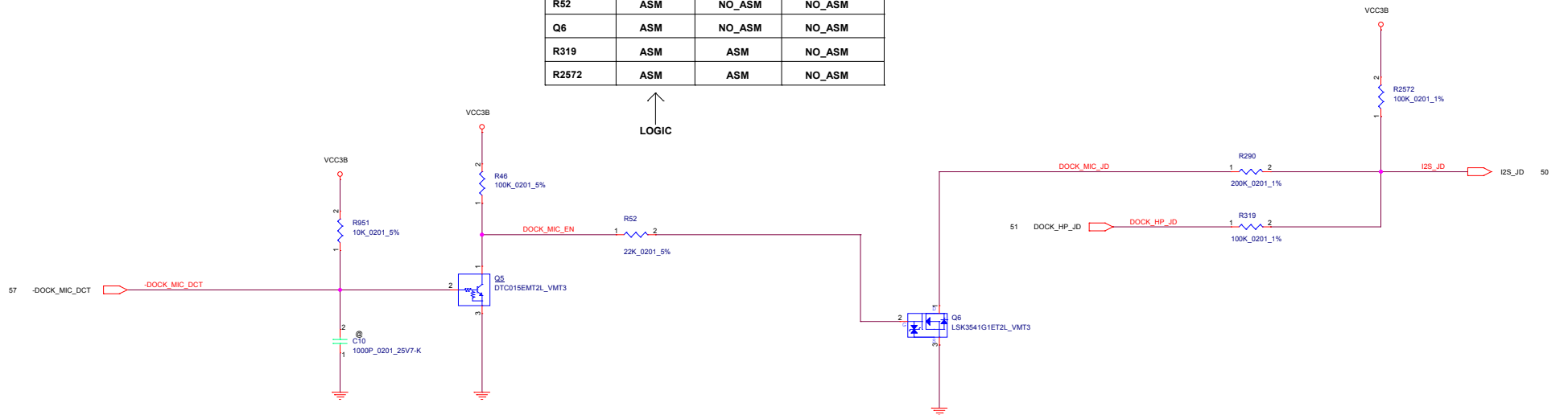




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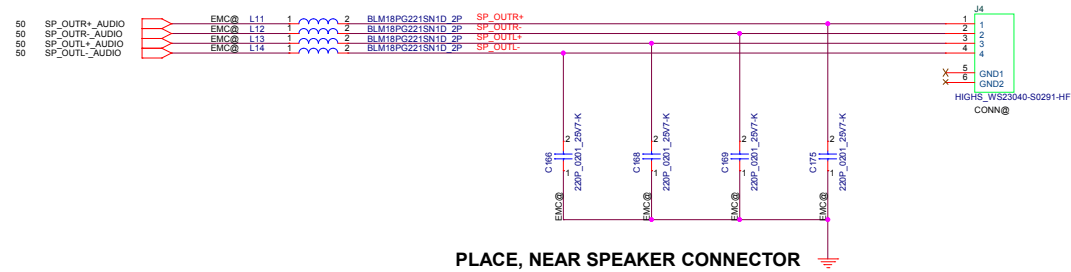
DOCKING	SUPPORT		NON-SUPPORT
	ENABLE	DISABLE	
R951	ASM	NO_ASM	NO_ASM
R290	ASM	NO_ASM	NO_ASM
R46	ASM	NO_ASM	NO_ASM
Q5	ASM	NO_ASM	NO_ASM
R52	ASM	NO_ASM	NO_ASM
Q6	ASM	NO_ASM	NO_ASM
R319	ASM	ASM	NO_ASM
R2572	ASM	ASM	NO_ASM

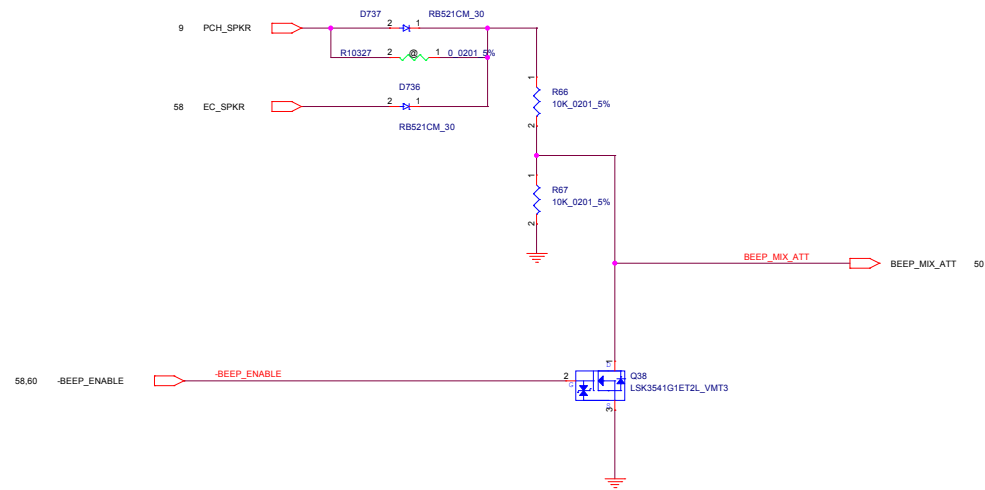
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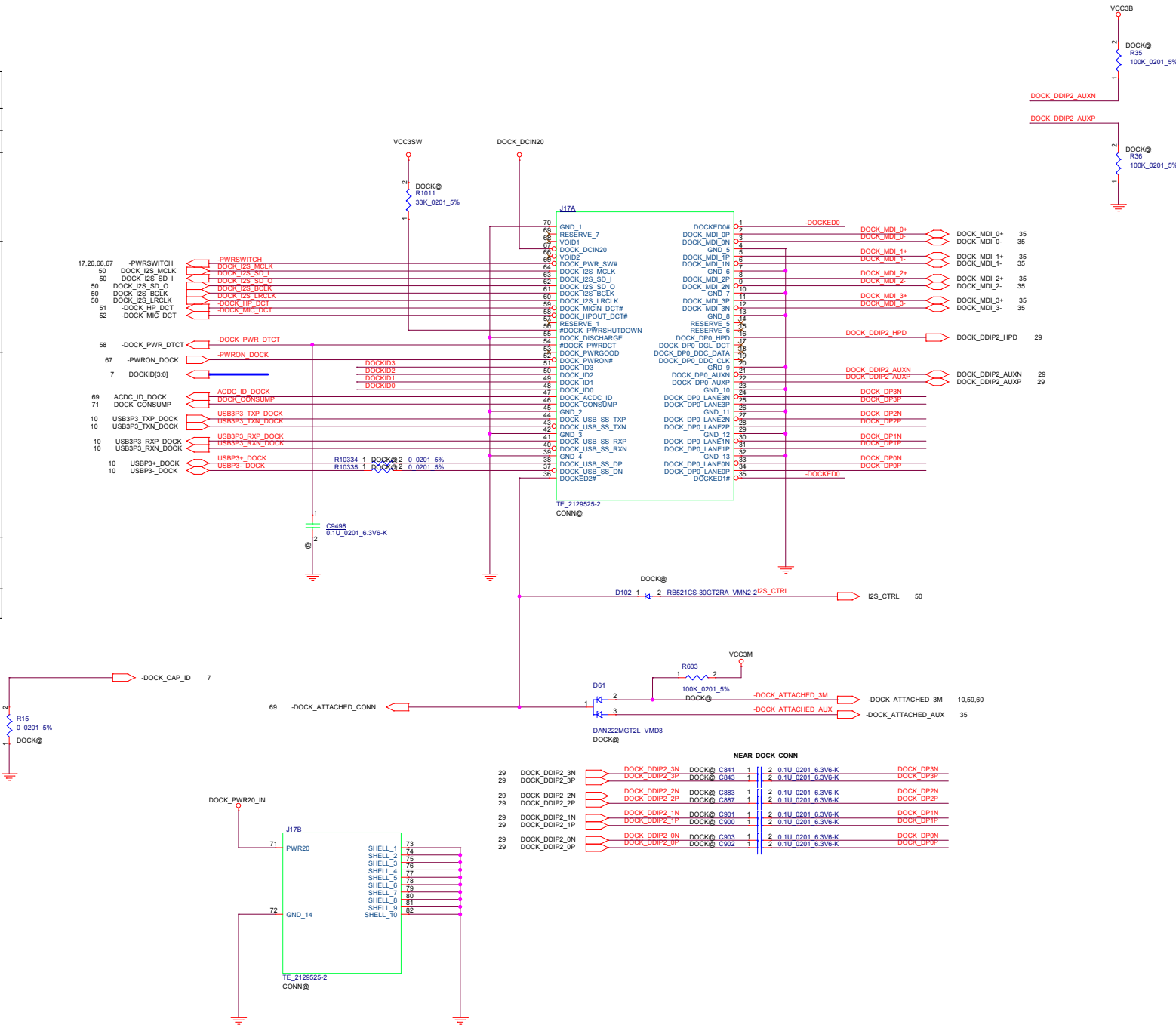
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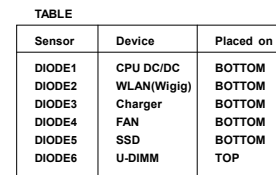
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TABLE		
ID	DOCKING SUPPORT	NON-SUPPORT
J17	ASM	NO ASM
R1011	ASM	NO ASM
D2	ASM	NO ASM
R603	ASM	ASM
D61	ASM	NO ASM
D102	ASM	NO ASM
C24	ASM	NO ASM
Q85	ASM	NO ASM
R95	ASM	NO ASM
R731	ASM	NO ASM
R657	ASM	NO ASM
C841	ASM	NO ASM
C843	ASM	NO ASM
C883	ASM	NO ASM
C887	ASM	NO ASM
C901	ASM	NO ASM
C900	ASM	NO ASM
C903	ASM	NO ASM
C902	ASM	NO ASM
R35	ASM	NO ASM
R36	ASM	NO ASM
R15	ASM	NO_ASM





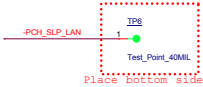
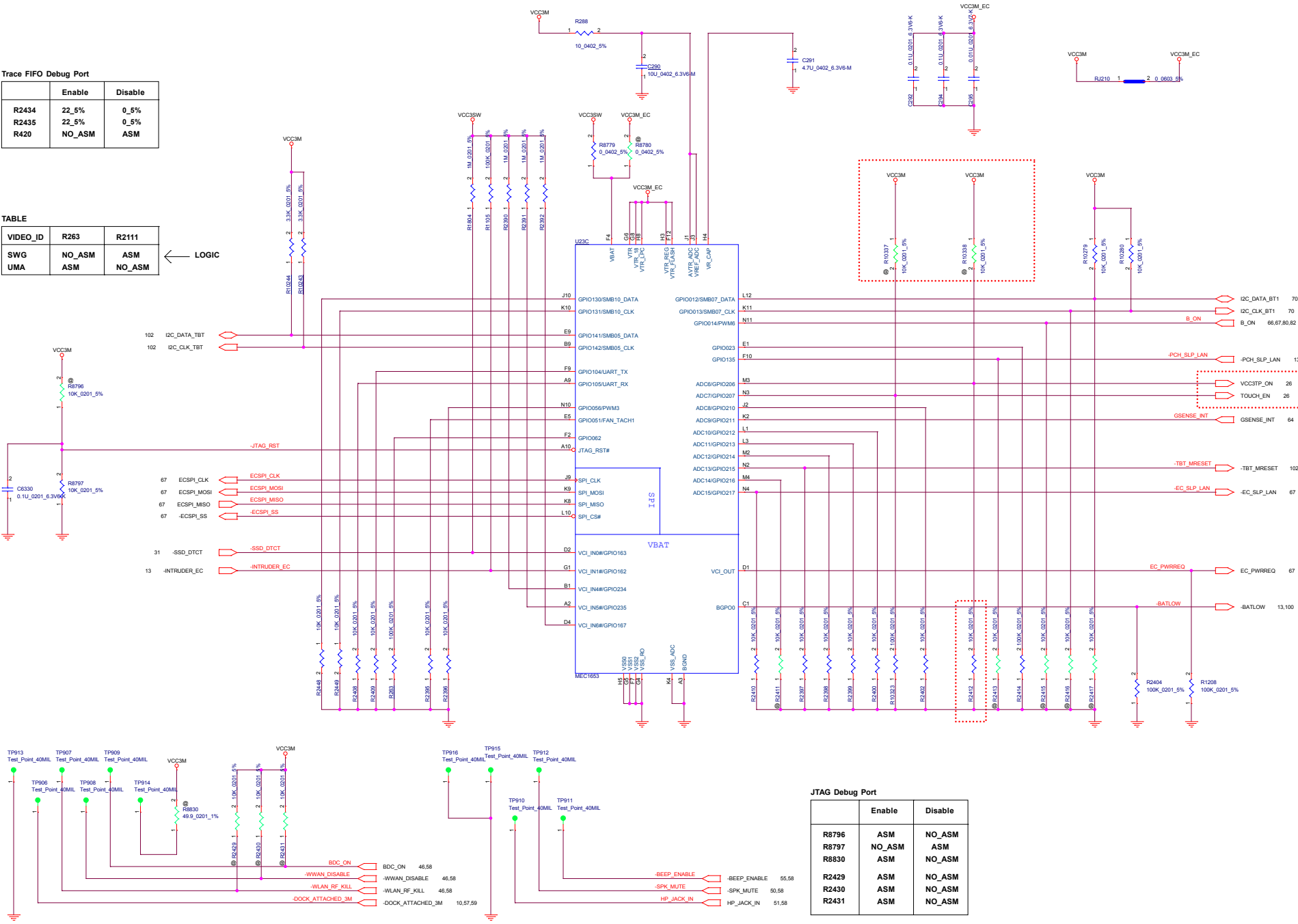
Trace FIFO Debug Port

	Enable	Disable
R2434	22_5%	0_5%
R2435	22_5%	0_5%
R420	NO_ASM	ASM

TABLE

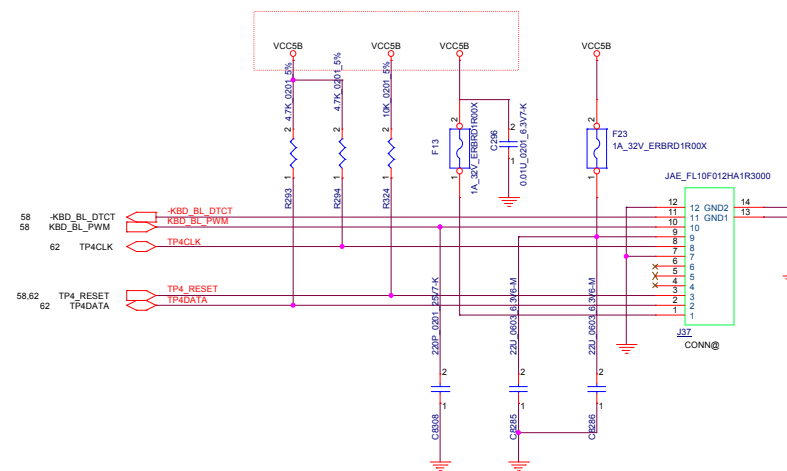
VIDEO_ID	R263	R2111
SWG	NO_ASM	ASM
UMA	ASM	NO_ASM


← LOGIC

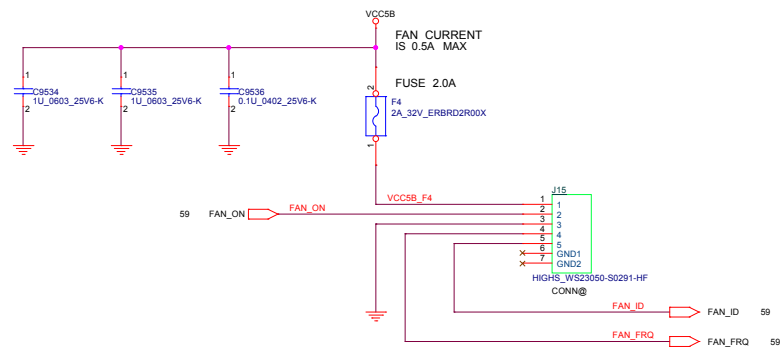


JTAG Debug Port

	Enable	Disable
R8796	ASM	NO_ASM
R8797	NO_ASM	ASM
R8830	ASM	NO_ASM
R2429	ASM	NO_ASM
R2430	ASM	NO_ASM
R2431	ASM	NO_ASM



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P/N	ADDR_SEL	Address
KX023-1025	H L	3Eh (W) & 3Fh (R) 3Ch (W) & 3Dh (R)

P/N	Mode Selection
H	I2C Mode
L	SPI Mode

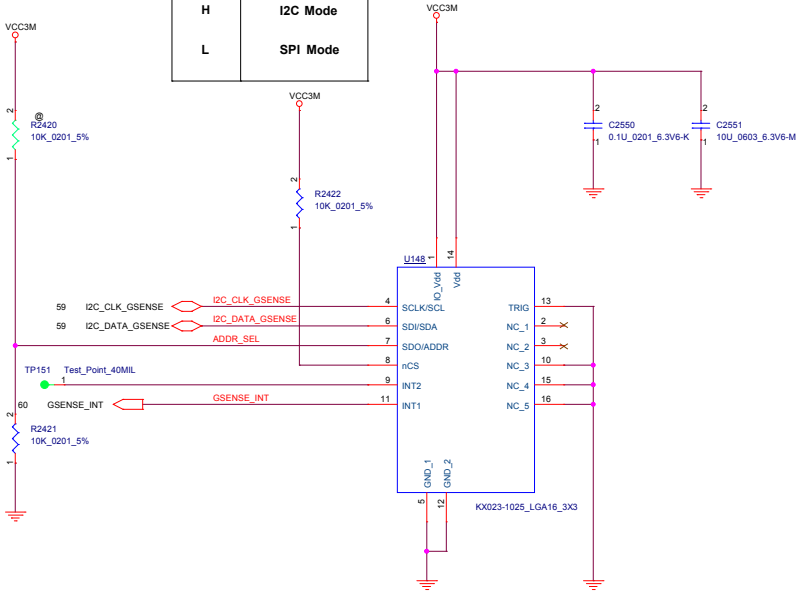
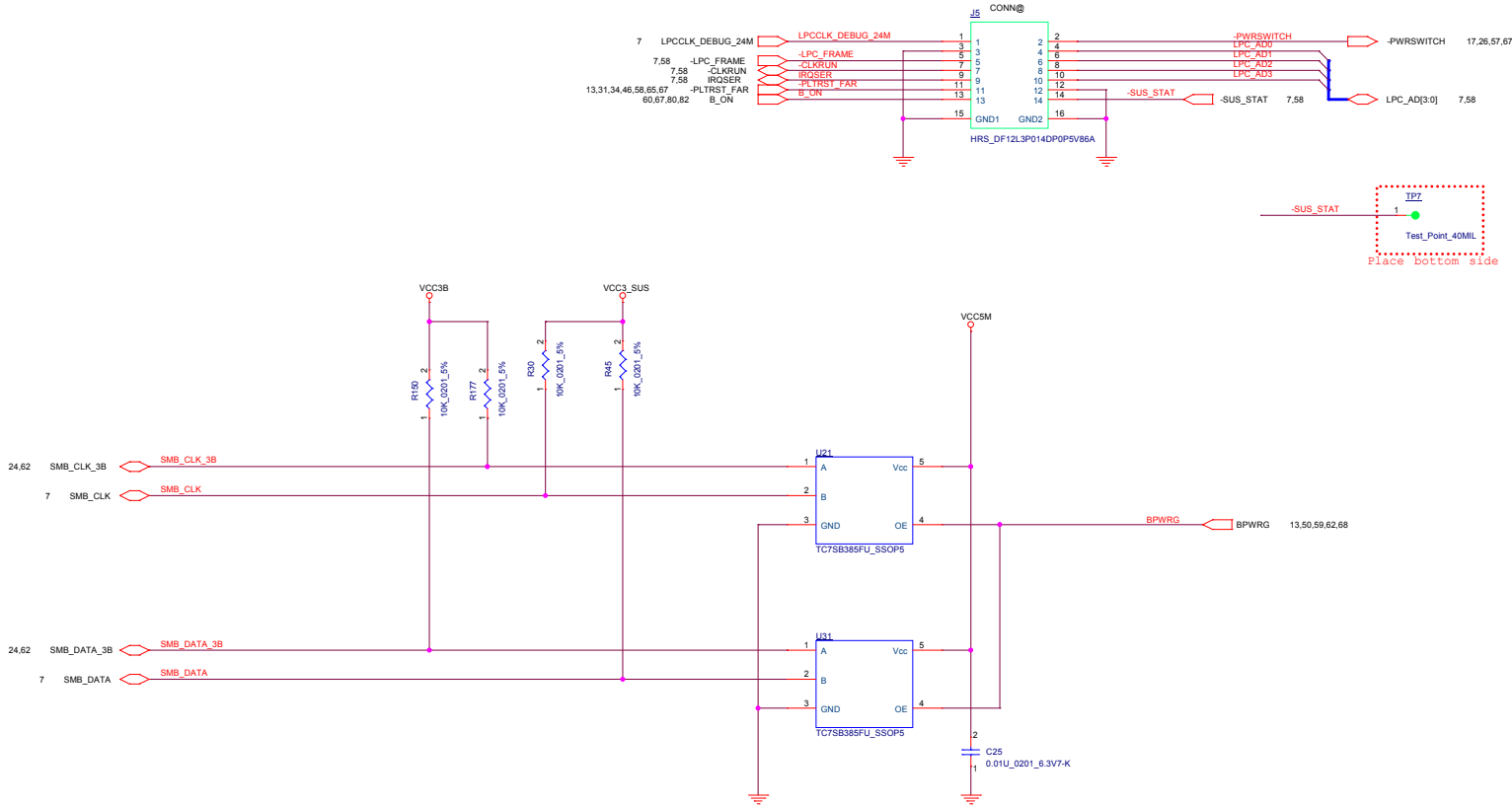
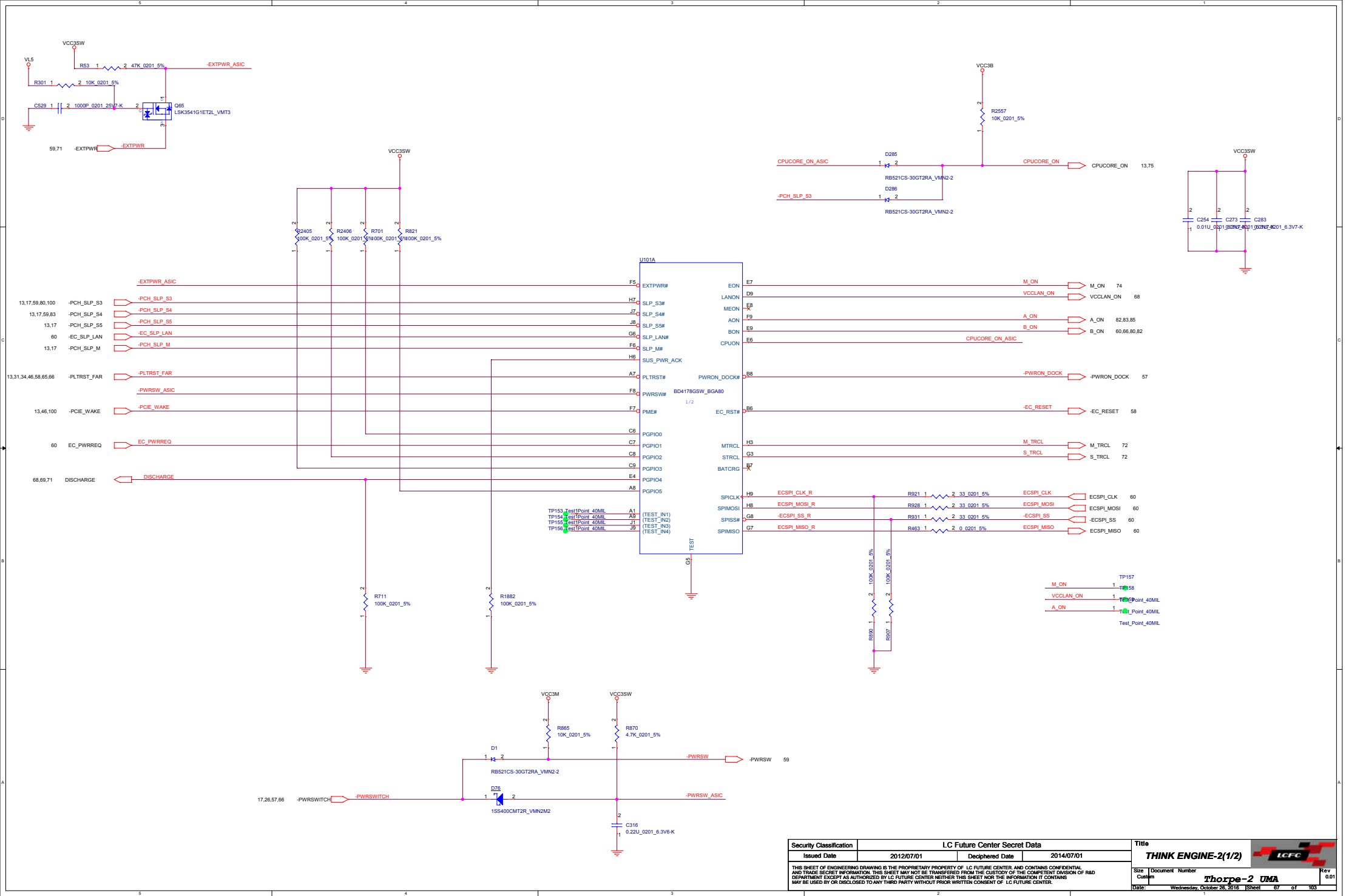


TABLE		
REF DES	ENABLE	DISABLE
J5	ASM	NO_ASM
R220	ASM	NO_ASM

LOGIC

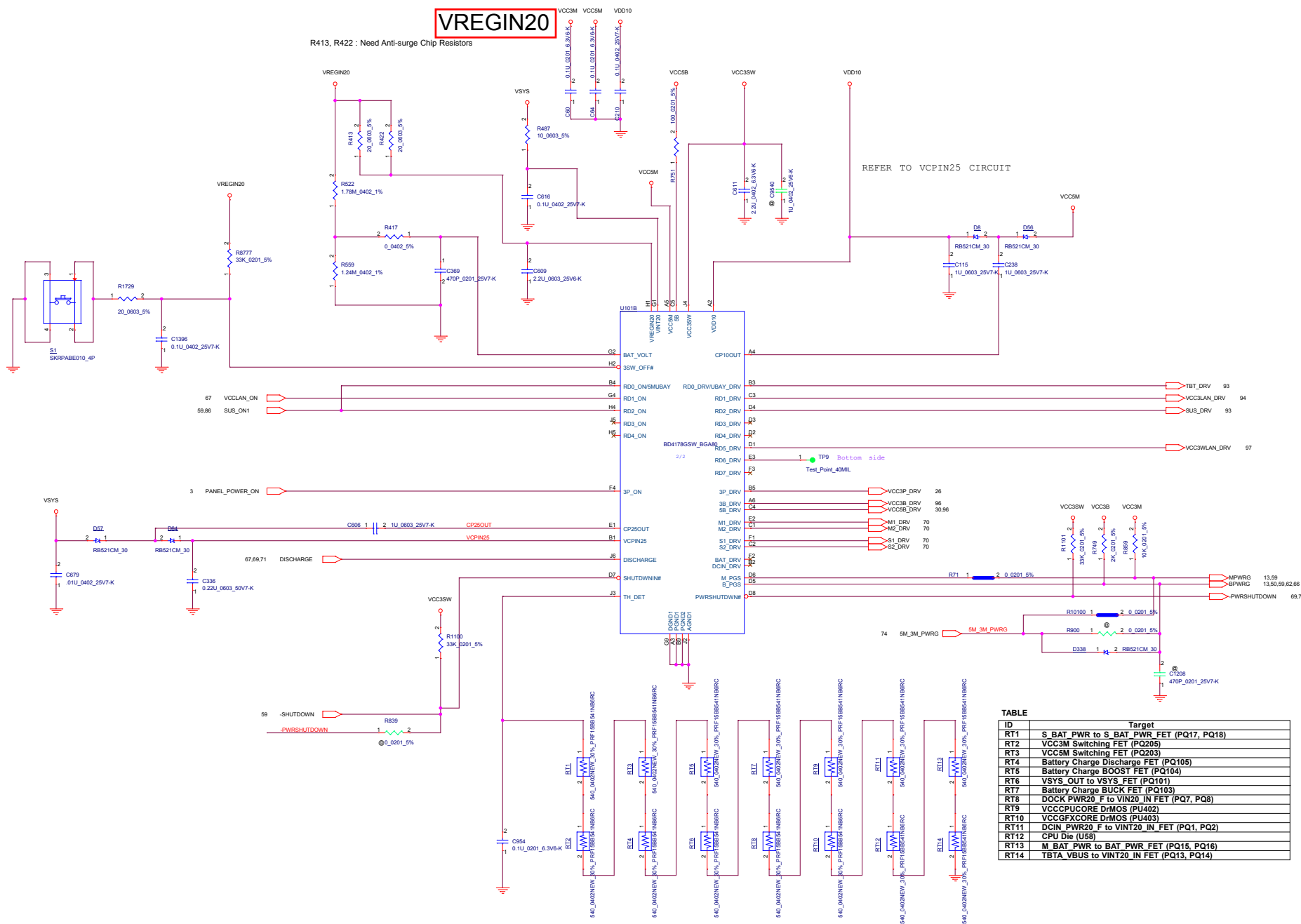
SDV staff



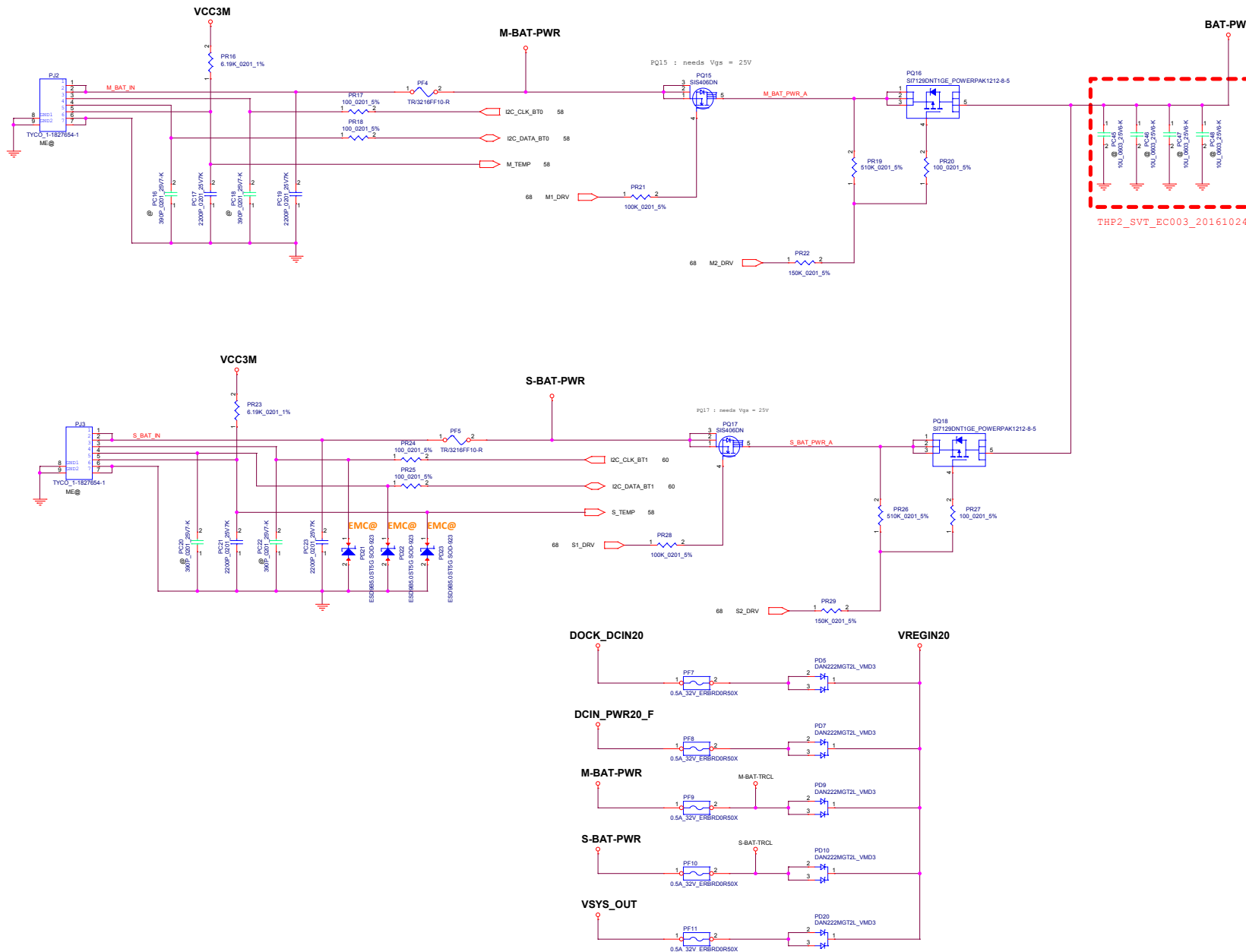


VREGIN20

R413, R422 : Need Anti-surge Chip Resistors



ID	Target
RT1	S BAT PWR to S BAT PWR FET (PQ17, PQ18)
RT2	VCC3M Switching FET (PQ205)
RT3	VCC5M Switching FET (PQ203)
RT4	Battery Charge Discharge FET (PQ105)
RT5	Battery Charge BOOST FET (PQ104)
RT6	VSYS_OUT to VSYS FET (PQ101)
RT7	Battery Charge BUCK FET (PQ103)
RT8	DOCK PWR20_F to VIN20_IN FET (PQ7, PQ8)
RT9	VCC3PUCORE DrMOS (PU402)
RT10	VCC3PUCORE DrMOS (PU403)
RT11	DCIN_PWR20_F to VINT20_IN FET (PQ1, PQ2)
RT12	CPU Die (U58)
RT13	M BAT PWR to BAT PWR FET (PQ15, PQ16)
RT14	TBTA_VBUS to VINT20_IN FET (PQ13, PQ14)



VINT20_IN MLCCs must be placed symmetrically on Top and Bottom.

Keep these two signals as pair routing

Should be placed near ACP, ACN

Keep these two signals as pair routing

IDPM	V (ILIM)	PR131
500mA	1.2V	402K
1.0A	1.4V	332K
1.5A	1.6V	280K
2.0A	1.8V	237K
3.0A	2.2V	174K
3.25A	2.3V	162K

← LOGIC

Table PL101
TOKO: FDS0630-H-2R2M
Cyntec: CMLE063T-2R2MS

MLCCs must be placed symmetrically on Top and Bottom.

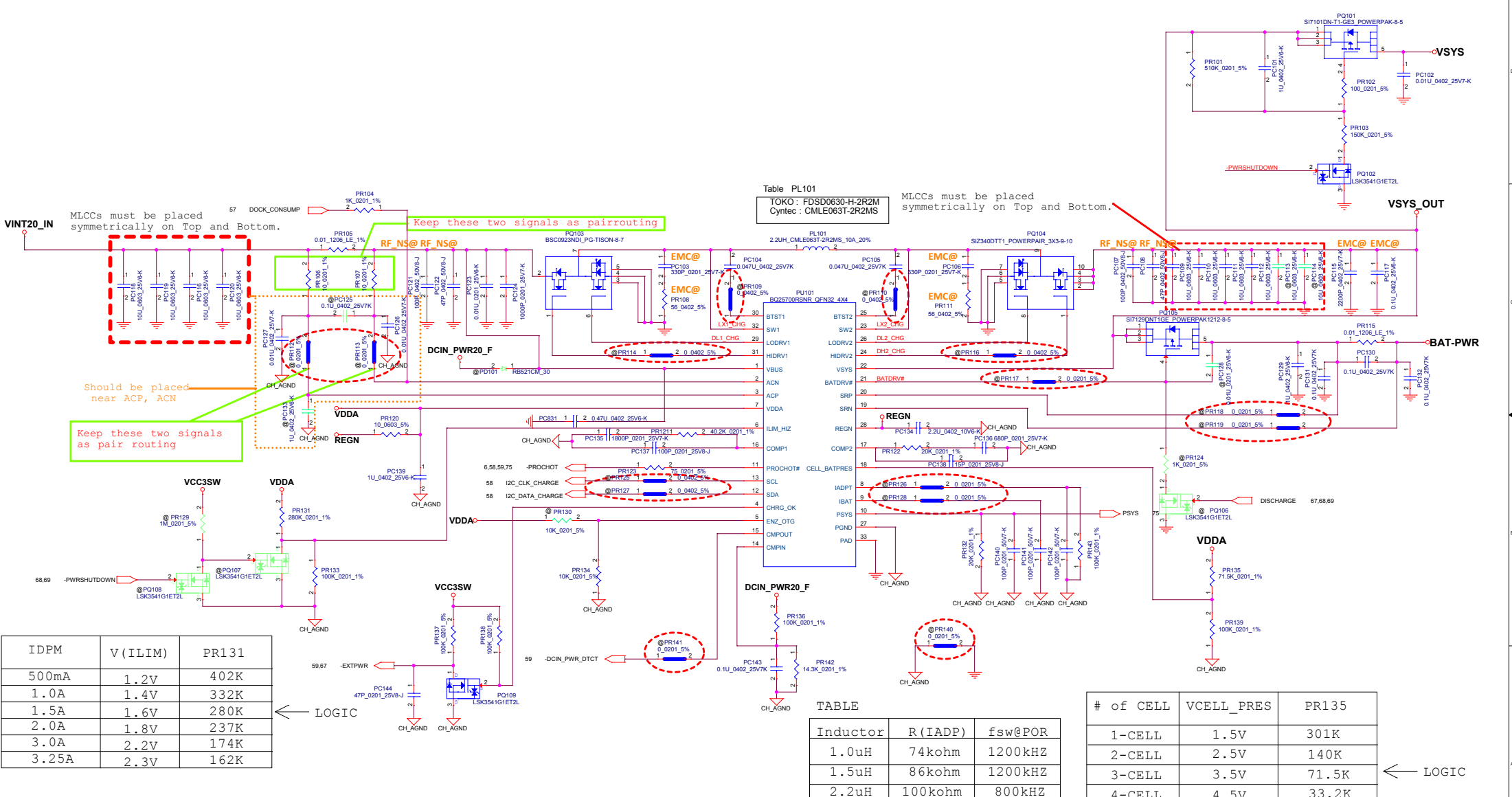
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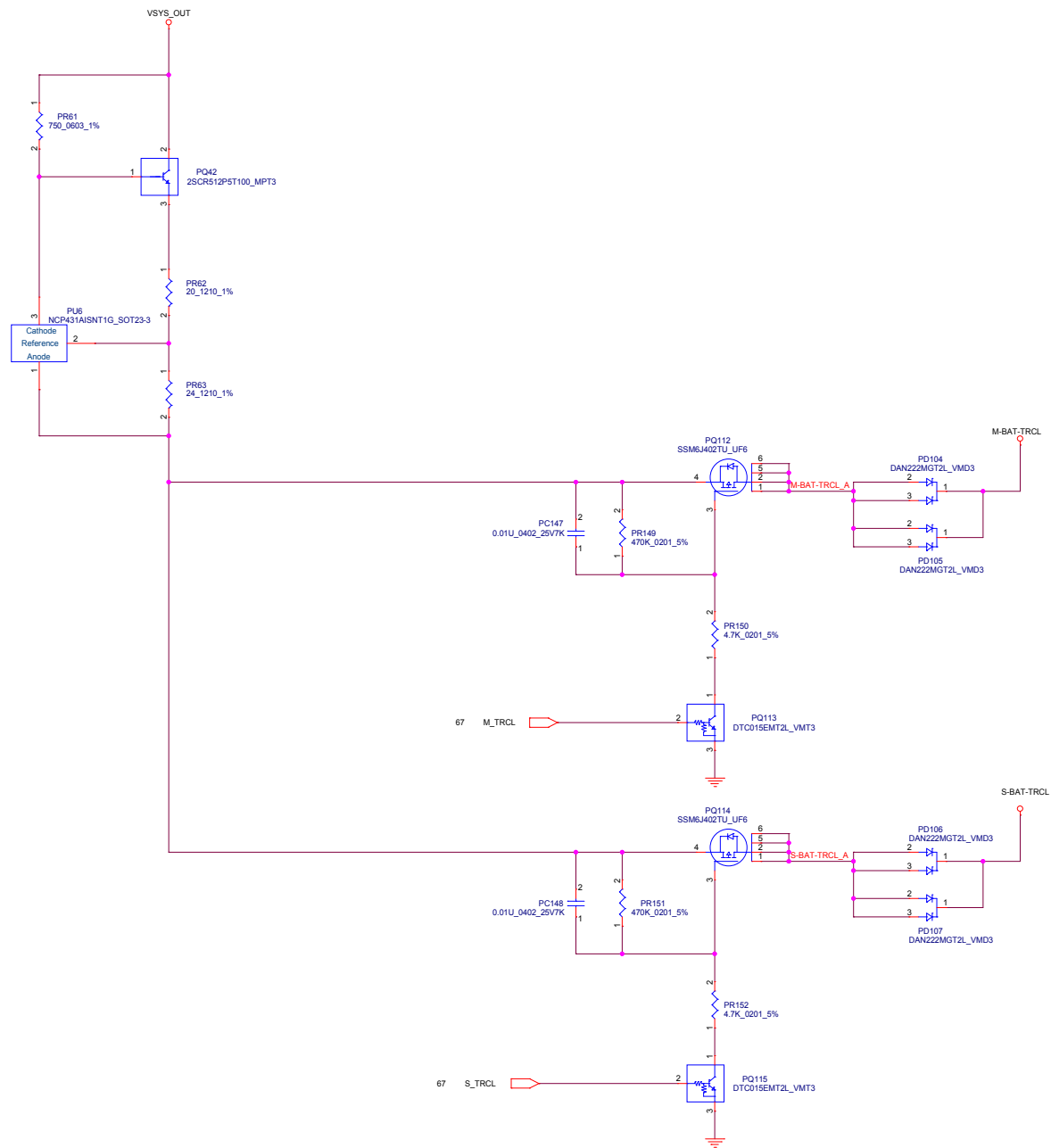
Inductor	R (IADP)	fs@POR
1.0uH	74kohm	1200kHz
1.5uH	86kohm	1200kHz
2.2uH	100kohm	800kHz

# of CELL	VCELL Pres	PR135
1-CELL	1.5V	301K
2-CELL	2.5V	140K
3-CELL	3.5V	71.5K
4-CELL	4.5V	33.2K

← LOGIC

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All the input MLCCs on 20V must be placed symmetrically on Top and Bottom.

VSYS

11A (TDC=9A) VCC5M

Table PL201

TDK: SPM6530T-1R5M100
Cyntec: CMLE0630T-1R5MS

Table PL202

TDK: SPM6530T-1R5M100
Cyntec: CMLE0630T-1R5MS


Table PC218, PC222, PC223

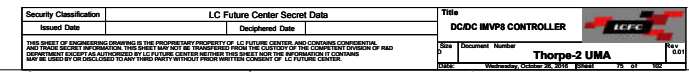
Panasonic: 6TPE220MAPB
NEC-TOKIN: TEPSLB20J227M(25)B/R

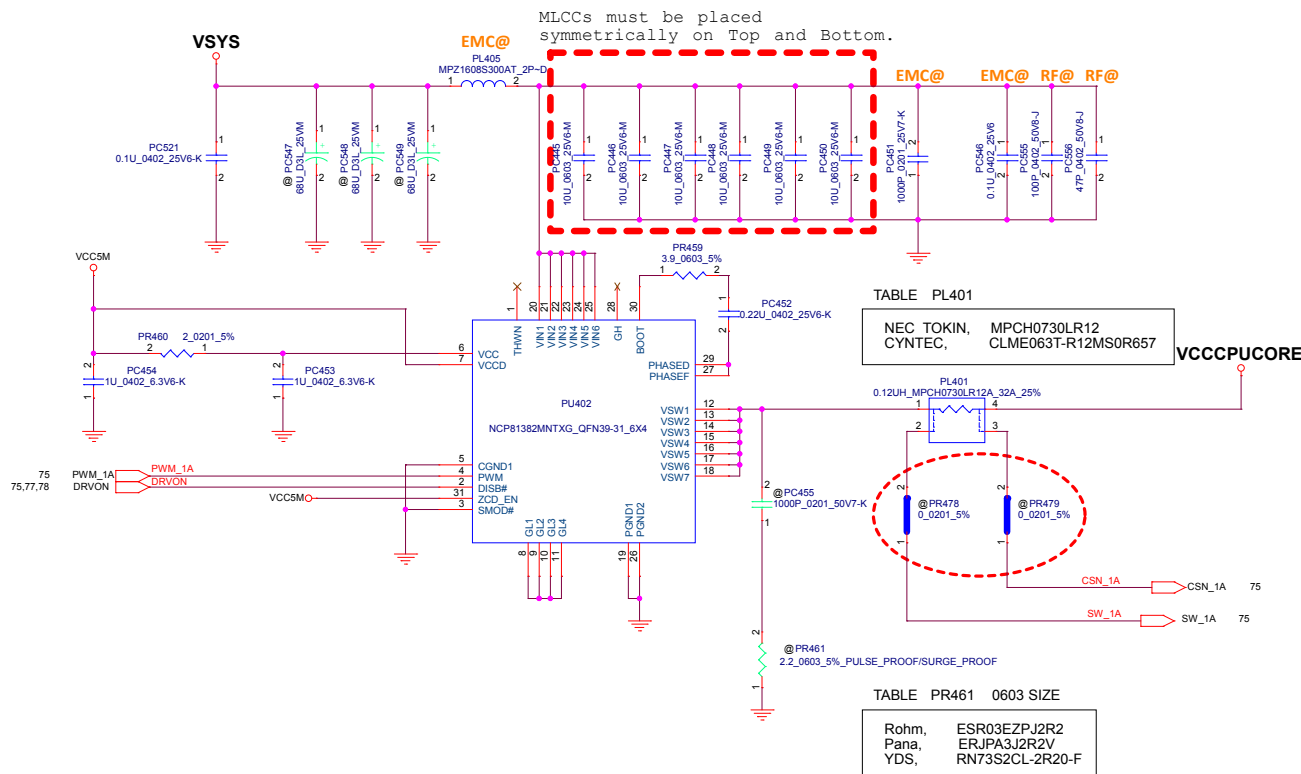
Table PC220, PC221, PC232

Panasonic: 6TPE220MAPB
NEC-TOKIN: TEPSLB20J227M(25)B/R

All the input MLCCs on 20V must be placed symmetrically on Top and Bottom.

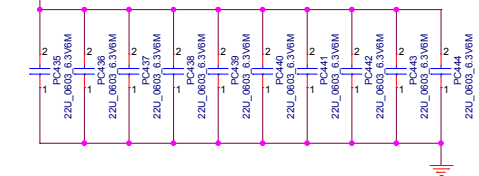
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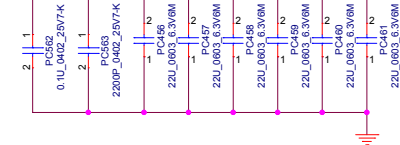
VCCCPUCORE

20pcs 22uF for VCCCPUCORE



VCCCPUCORE

EMC@ EMC@



VCCCPUCORE

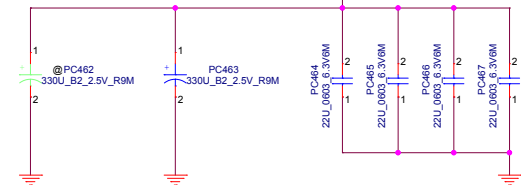
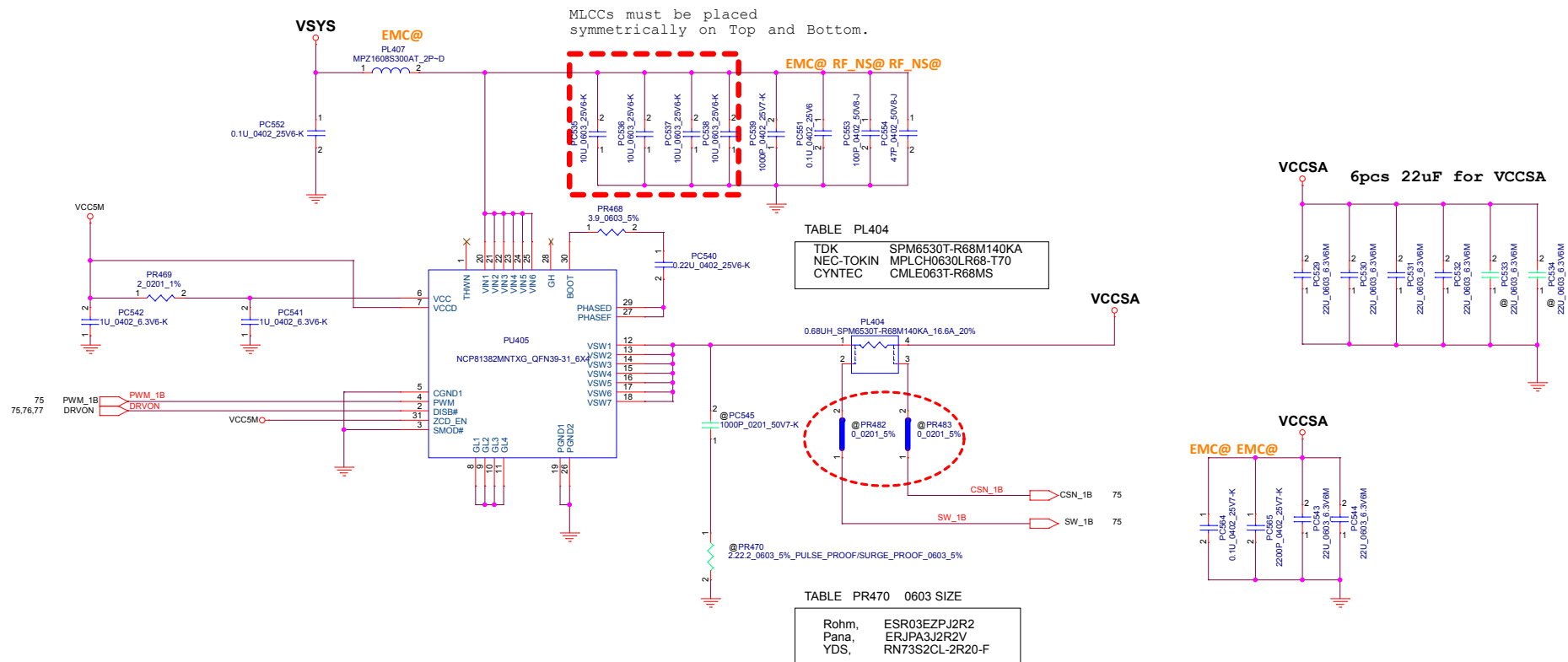



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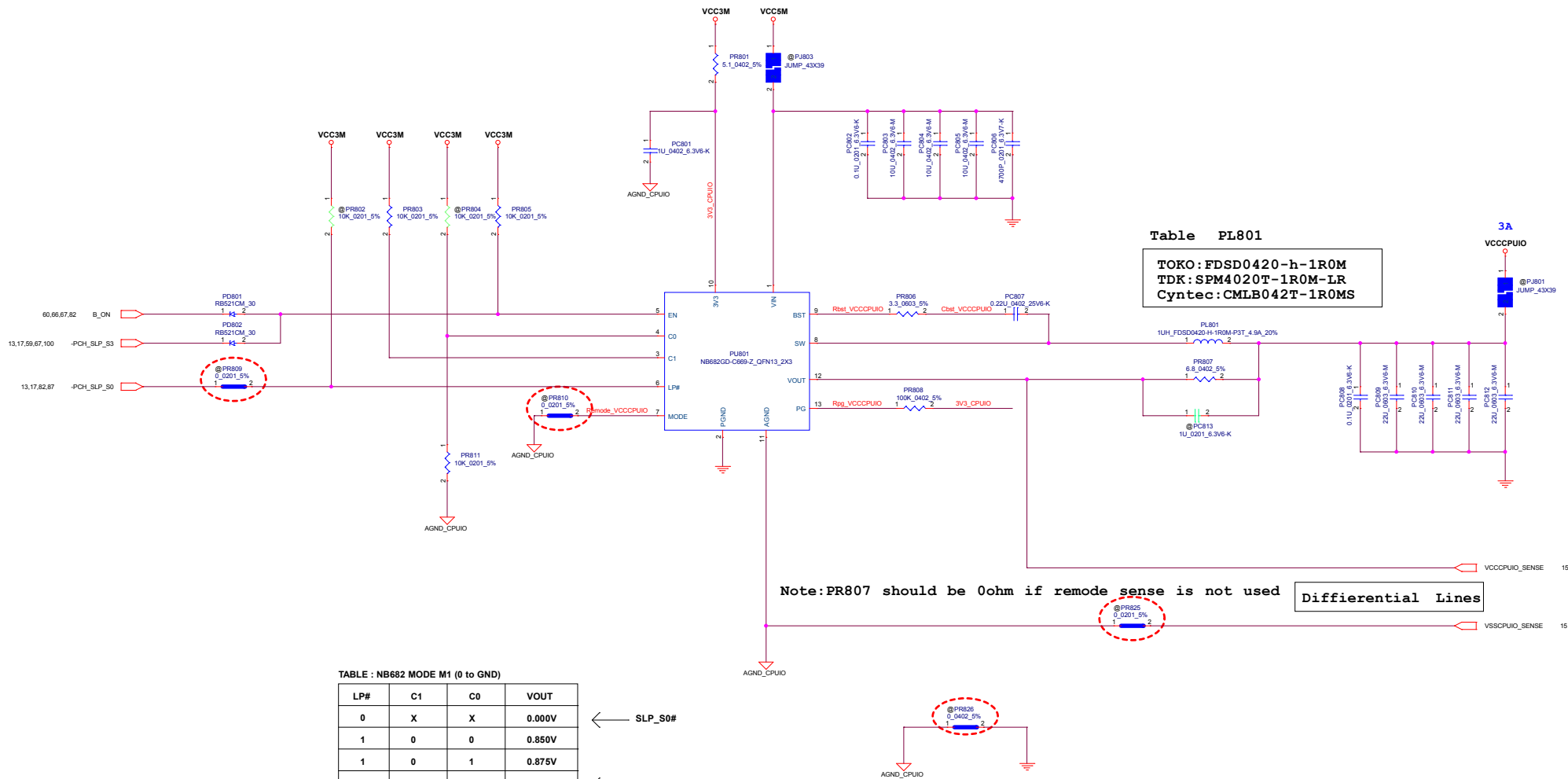
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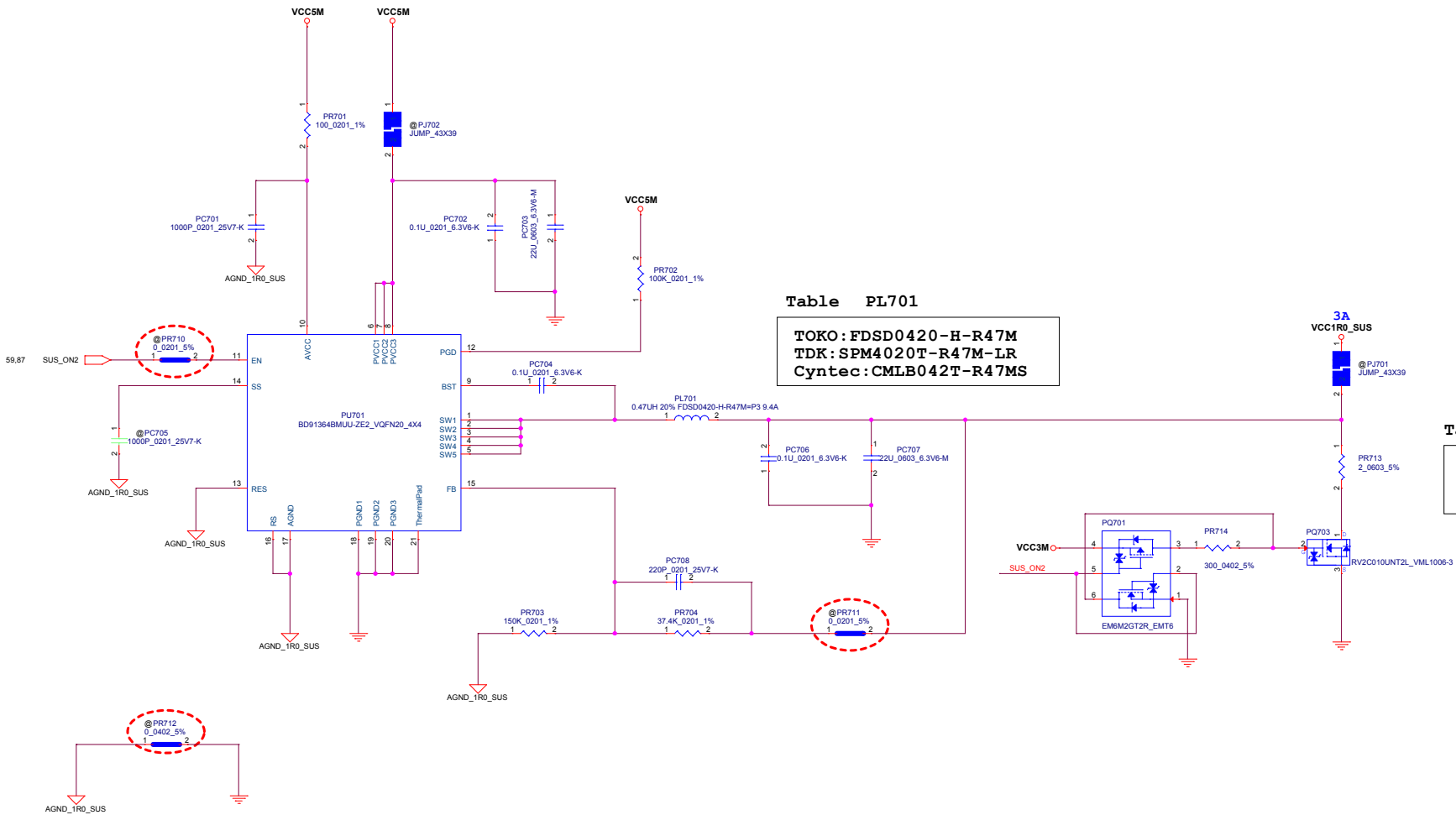


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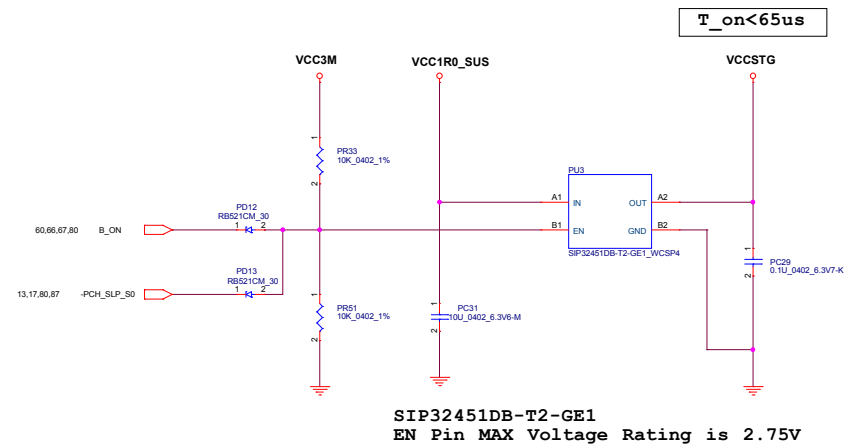
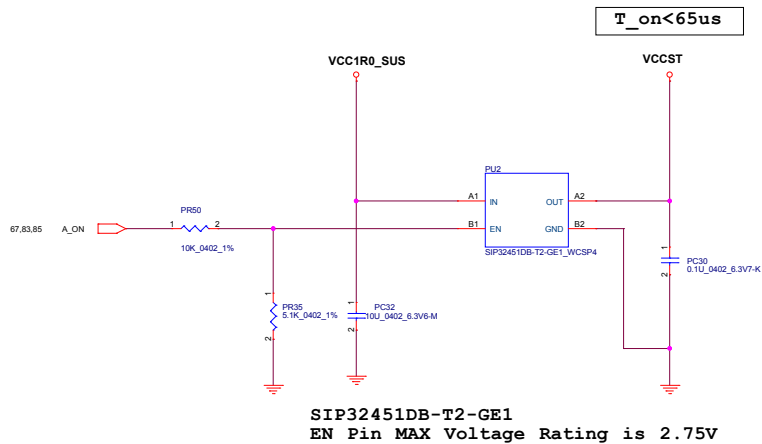
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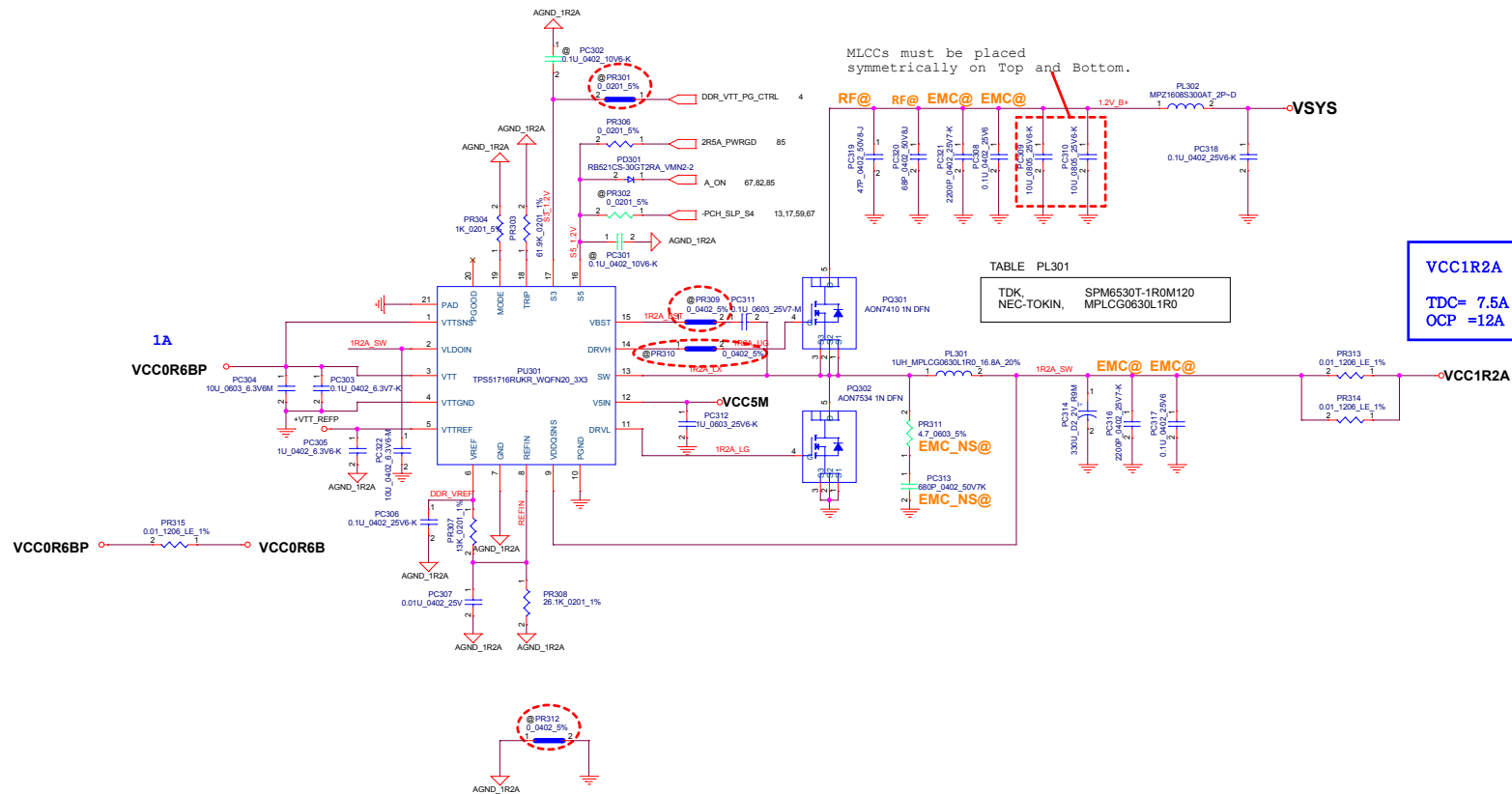
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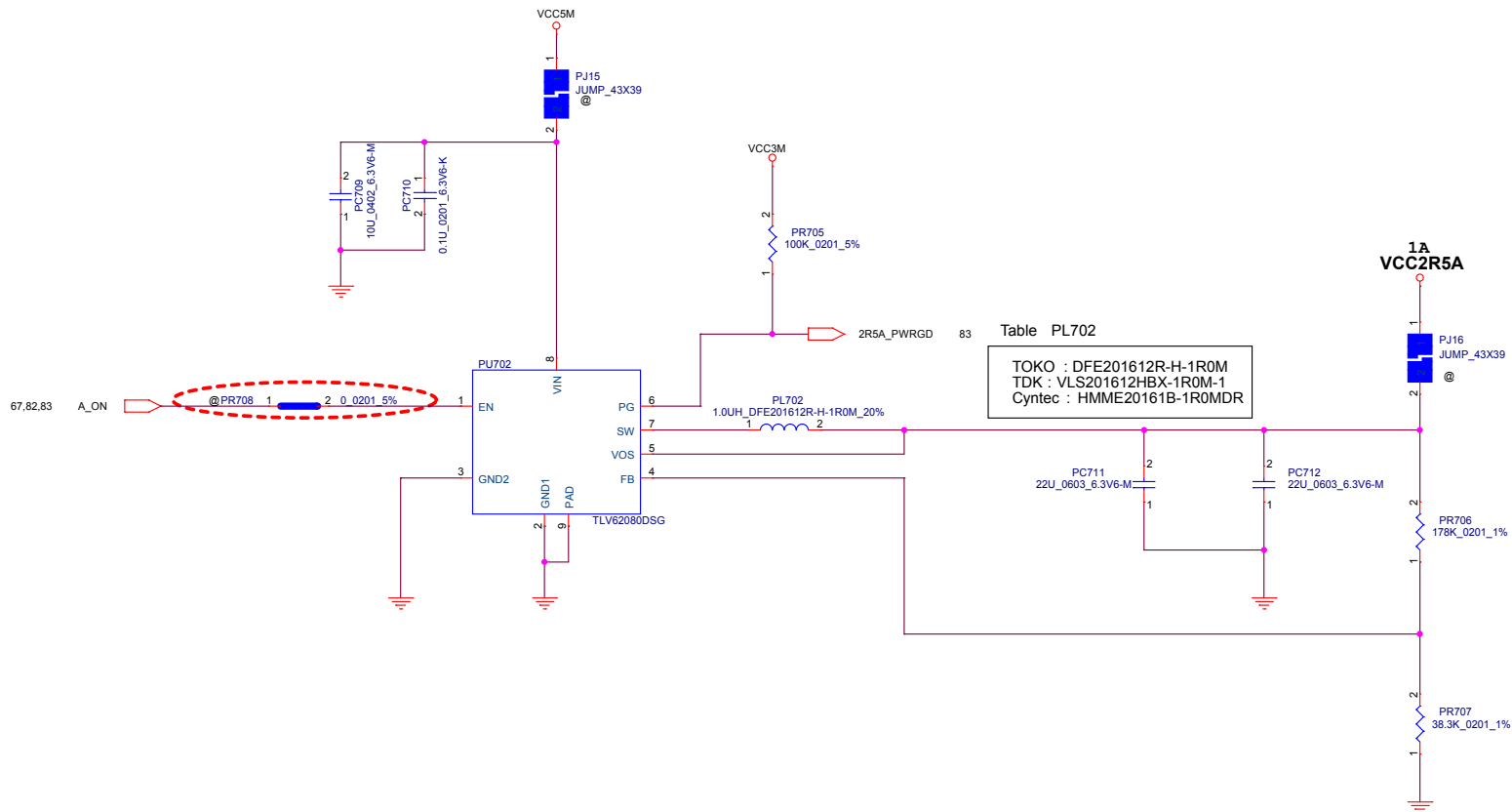



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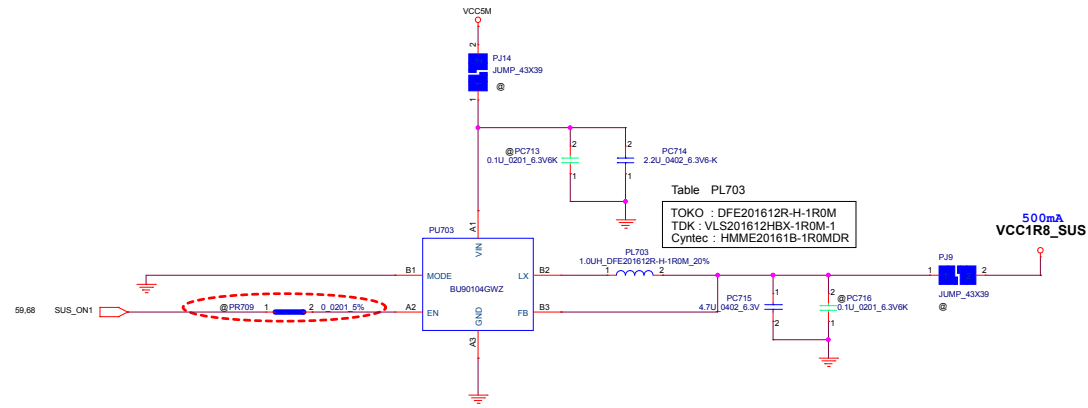


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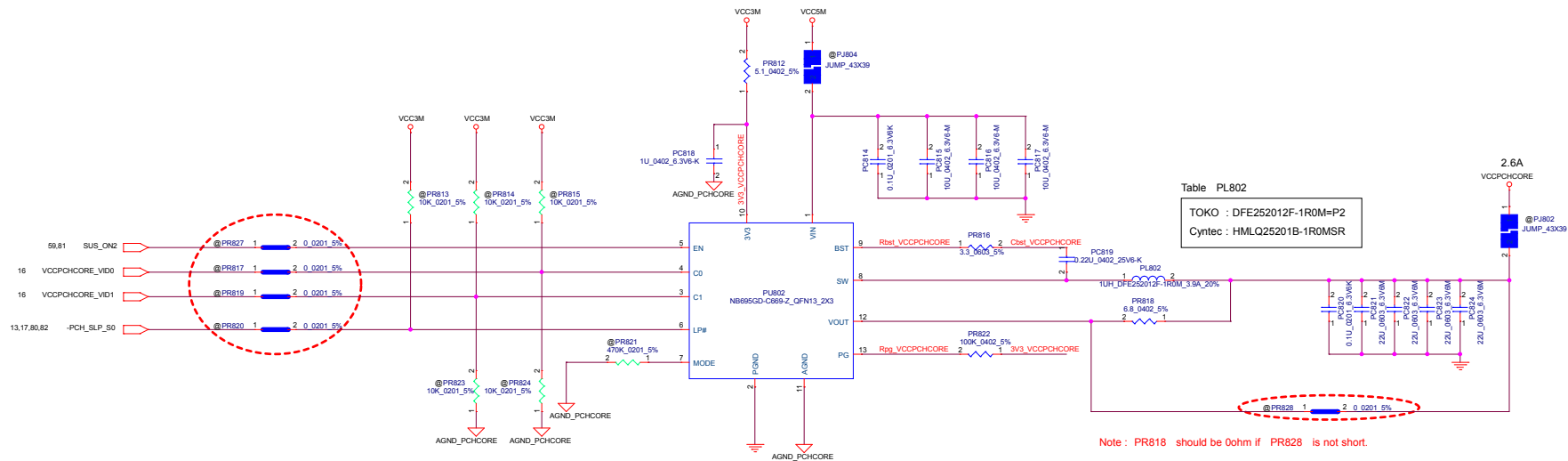


TABLE : NB695 MODE M2 (Float)


LP#	C1	C0	VOUT
0	X	X	0.700V
1	0	0	0.850V
1	0	1	0.900V
1	1	0	0.950V
1	1	1	1.000V

← SLP_S0#


← DEFAULT




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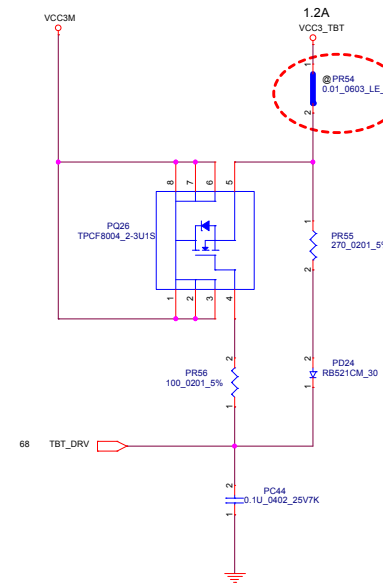
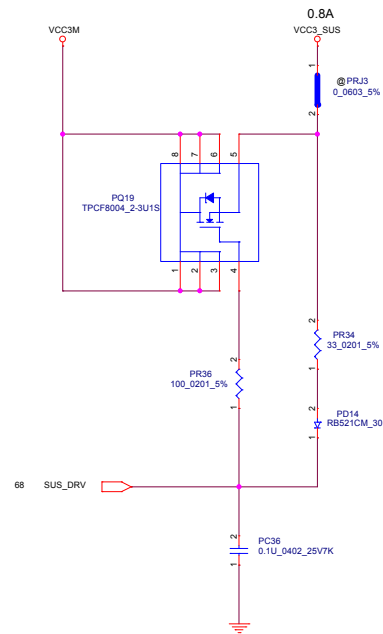
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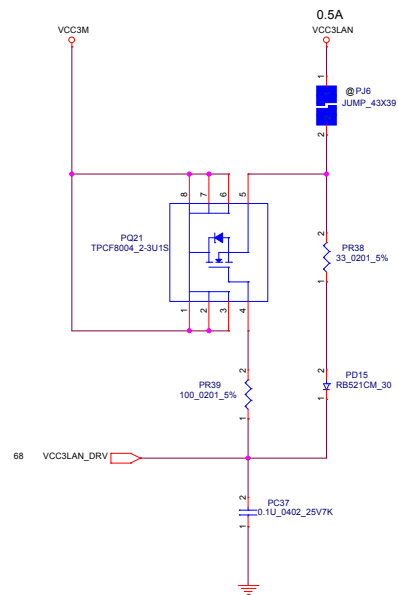
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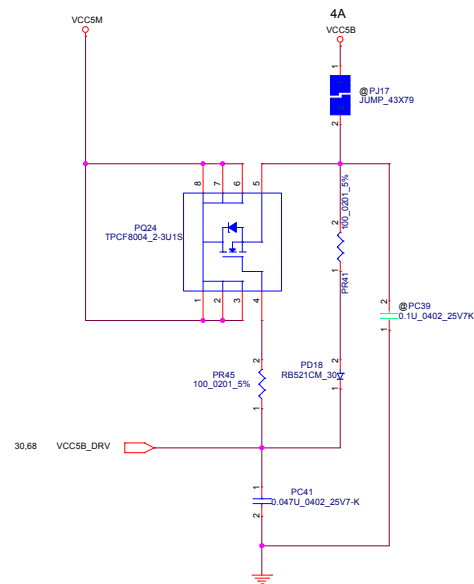
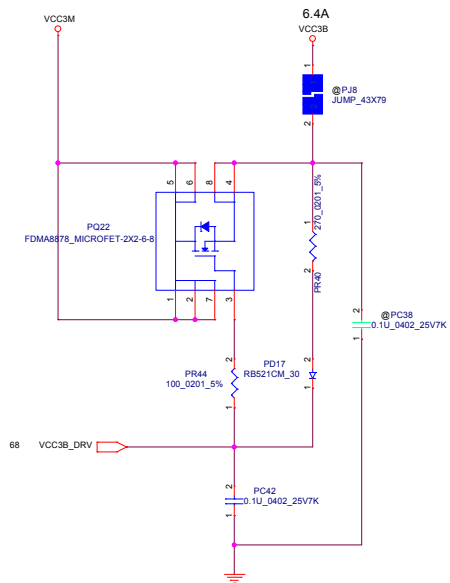
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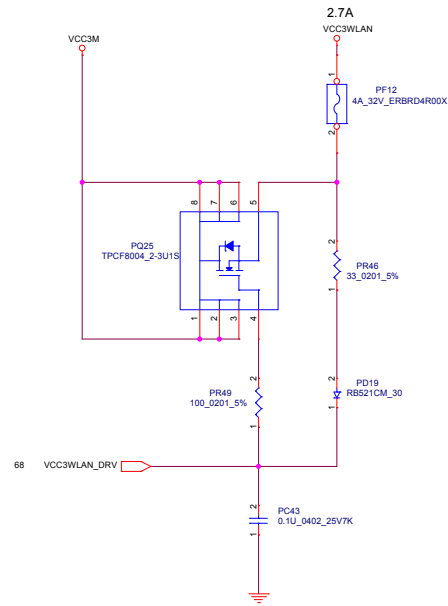
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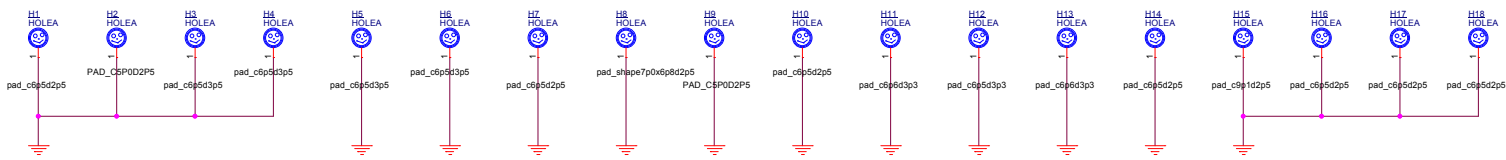
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PC8283	ASM	NO-ASM
PD238	ASM	NO-ASM

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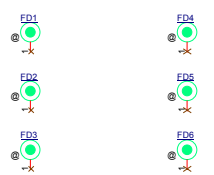


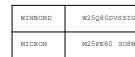



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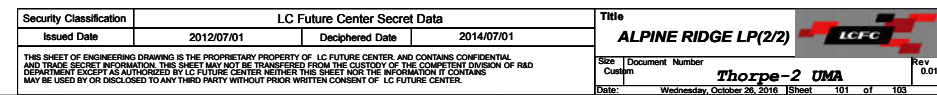


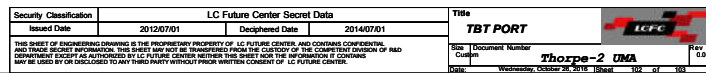
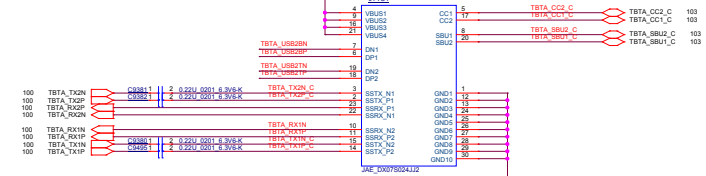
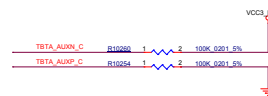
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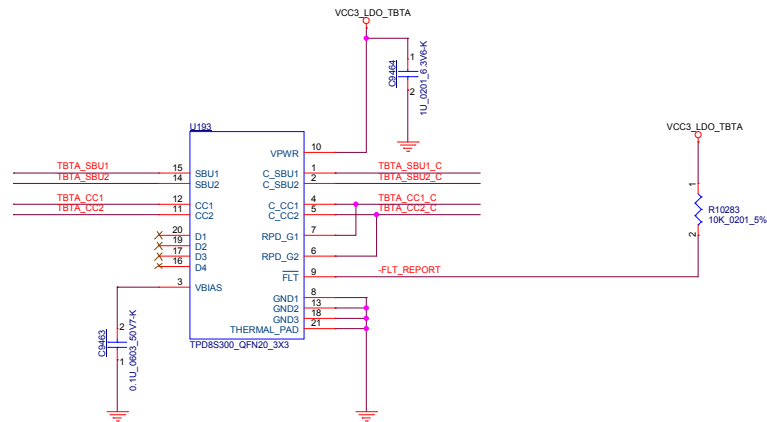




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